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     FILE 'WPIX, JAPIO' ENTERED AT 10:59:07 ON 27 SEP 2002
L1          6757 S BALL()GRID OR BALLGRID? OR BGA OR BGAS OR PBGAS OR PBGA OR CG
L2          8832 S (SOLDER OR SOLDERING OR SOLDERED OR BRAZ?)(2N)(BALL OR BALLS
L3        150875 S (HEAT? OR WARM? OR HOT OR THERMOL? OR THERMAL? OR PREHEAT? OR
L4        138506 S (CIRCUIT)(2N)(BOARD) OR SYSTEM()BOARD OR MOTHERBOARD
L5        158329 S SOLDER OR SOLDERING OR SOLDERED OR BRAZ?
L6           515 S V04-R06D3/MC
L7        875591 S IC OR ICS OR ((INTEGRATED OR LOGIC)(W)(CIRCUIT?)) OR (MICRO)(
L8         24049 S (CONTACT? OR BONDING)(2N)(PAD OR PADS OR BUMP OR BUMPS)
L9         34676 S (WIRE OR WIRES OR LINE OR LINES)(2N)(BOND?)
L10         6910 S U11-E01A/MC
L11        54876 S (H01L-021/60 OR H01L-021/603 OR H01L-021/607)/IC
L12         4319 S (CONDUCTIV?)(3N)(BUMP? OR PAD OR PADS)
L13          203 S L1 AND L3
L14           13 S L13 AND STIFFENER
L15          102 S L1 AND STIFFENER
L16            9 S L15 AND (PCB OR L4)
L17            9 S L16 NOT L14
L18           77 S L13 AND (METAL OR COPPER OR CU OR ALUMINUM OR AL OR ALUMINIUM
L19           22 S L18 AND L2
L20           21 S L19 NOT (L14 OR L16)
L21           19 S L13 AND THERMAL?()CONDUCTIV?
L22           17 S L13 AND L8
L23            1 S L13 AND WINDOW
L24           34 S (L21 OR L22) NOT (L14 OR L16 OR L23)
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L14 ANSWER 1 OF 13 WPIX (C) 2002 THOMSON DERWENT
AN 2001-538652 [60] WPIX
DNN N2001-400266 DNC C2001-160416
TI Multilayered TAB tape for **BGA** package used in PC, is attached to **stiffener** by thermosetting adhesive layer having specific thickness and hardness.
DC A85 L03 U11
PA (HITD) HITACHI CABLE LTD
CYC 1
PI JP 2001068512 A 20010316 (200160)* 7p
ADT JP 2001068512 A JP 1999-241524 19990827
PRAI JP 1999-241524 19990827
AB JP2001068512 A UPAB: 20011018
NOVELTY - The blackening oxide film (4) and the black epoxy resin layer (1) are formed on both surfaces of **stiffener** (2). The TAB tape (15) has copper laminate (8) and the insulating layer (6) that are bonded by adhesive layer (7). The **stiffener** and TAB tape are bonded by a thermosetting adhesive layer (5) having hardness as 1 multiply 105 dyns2 and thickness of 30-50 mu m.
DETAILED DESCRIPTION - An INDEPENDENT CLAIM is also included for **BGA** package.
USE - For **BGA** package used in PC, high-speed digital data processor.
ADVANTAGE - Improves heat release property of **stiffener**, by **covering heat** release face by black epoxy resin layer. Improves wire bonding characteristic, by eliminating absorption of vibrational energy during wire bonding. Improves solder reflow characteristic, by reducing heat release by **stiffener** during reflow.
DESCRIPTION OF DRAWING(S) - The figure shows the cross-sectional view of TAB tape. (Drawing includes non-English language text).
Black epoxy resin layer 1
**Stiffener** 2
Oxide film 4
Thermosetting adhesive layer 5
Insulating layer 6
Adhesive layer 7
Copper laminate 8
TAB tape 15
Dwg.1/4

L14 ANSWER 2 OF 13 WPIX (C) 2002 THOMSON DERWENT
AN 2001-334533 [35] WPIX
DNN N2001-241381
TI Structural configuration of electronic device e.g. flip chip package, includes electrically conductive material formed on portion of substrate top, that surrounds chip and substantially covers opposed side of chip.
DC U11
IN HOANG, L H
PA (LSIL-N) LSI LOGIC CORP
CYC 1
PI US 6201301 B1 20010313 (200135)* 8p
ADT US 6201301 B1 US 1998-10414 19980121
PRAI US 1998-10414 19980121
AB US 6201301 B UPAB: 20010625

NOVELTY - The active side of chip is electrically connected with substrate (10) top, while an underfill (36) that is resistive to electrical conduction is disposed between substrate top and chip active side. Electrically conductive material (30) comprising metal fillers, formed on a portion of substrate top, surrounds the chip and substantially covers the opposed side of chip.

USE - Electronic device e.g. flip chip **ball grid** array.

ADVANTAGE - As the electrically conductive material transfers heat from opposed side of chip, enhanced thermal performance is achieved. As **heat spreader** and **stiffener** are no more required, savings associated with cost of material and processing are achieved.

DESCRIPTION OF DRAWING(S) - The figure shows electrically conductive material covering top of opposed side of chip.

Substrate 10

Electrically conductive material 30

Underfill 36

Dwg.5/5

L14 ANSWER 3 OF 13 WPIX (C) 2002 THOMSON DERWENT
AN 2001-029262 [04] WPIX
DNN N2001-023273
TI Heat release metal plate for **ball grid** array ( **BGA**) type semiconductor device, includes **stiffeners** each formed by bending **spread**-out portion of **heat** sink and placing bent portion below heat sink.
DC U11
PA (NICH-N) NICHIDEN SEIMITSU KOGYO KK
CYC 1
PI JP 2000299417 A 20001024 (200104)* 11p
ADT JP 2000299417 A JP 1999-109490 19990416
PRAI JP 1999-109490 19990416
AB JP2000299417 A UPAB: 20010118

NOVELTY - The heat release metal plate (1) includes **stiffeners** (3) each formed by bending the spread-out portion of a heat sink (2) and placing the bent portion below the heat sink.

DETAILED DESCRIPTION - An INDEPENDENT CLAIM is also included for a semiconductor device manufacturing method.

USE - For **BGA** type semiconductor device.

ADVANTAGE - Reduces number of manufacturing processes for heat sink which functions both as **heat spreader** and **stiffener**. Simplifies manufacturing process since press formation does not need to be performed in metal plate except in heat sink and tape process for **stiffener** to heat sink is not required.

DESCRIPTION OF DRAWING(S) - The figure shows a sectional view of the heat release metal plate.

Heat release metal plate 1

Heat sink 2

**Stiffeners** 3

Dwg.1/10

L14 ANSWER 4 OF 13 WPIX (C) 2002 THOMSON DERWENT
AN 2000-490834 [43] WPIX
DNN N2000-364309 DNC C2000-147401
TI Electronic circuit device comprising a resin composition useful as an adhesive, covercoat or encapsulant contains an epoxy-modified aromatic

vinyl-conjugated diene block copolymer.

DC A12 A21 A85 L03 U11 V04

IN CLOUGH, R S

PA (MINN) 3M INNOVATIVE PROPERTIES CO

CYC 90

PI WO 2000039189 A1 20000706 (200043)* EN 44p
RW: AT BE CH CY DE DK EA ES FI FR GB GH GM GR IE IT KE LS LU MC MW NL OA PT SD SE SL SZ TZ UG ZW
W: AE AL AM AT AU AZ BA BB BG BR BY CA CH CN CR CU CZ DE DK DM EE ES FI GB GD GE GH GM HR HU ID IL IN IS JP KE KG KP KR KZ LC LK LR LS LT LU LV MD MG MK MN MW MX NO NZ PL PT RO RU SD SE SG SI SK SL TJ TM TR TT TZ UA UG UZ VN YU ZA ZW
AU 9962541 A 20000731 (200050)
US 6294270 B1 20010925 (200158)
EP 1141073 A1 20011010 (200167) EN
R: AT BE CH CY DE DK ES FI FR GB GR IE IT LI LU MC NL PT SE
US 2002001720 A1 20020103 (200207)
KR 2001099936 A 20011109 (200229)
CN 1337975 A 20020227 (200234)
US 6423367 B1 20020723 (200254)

ADT WO 2000039189 A1 WO 1999-US21592 19990916; AU 9962541 A AU 1999-62541 19990916; US 6294270 B1 US 1998-219265 19981223; EP 1141073 A1 EP 1999-949723 19990916, WO 1999-US21592 19990916; US 2002001720 A1 Div ex US 1998-219265 19981223, US 2001-917543 20010727; KR 2001099936 A KR 2001-708087 20010623; CN 1337975 A CN 1999-814898 19990916; US 6423367 B1 Div ex US 1998-219265 19981223, US 2001-917543 20010727

FDT AU 9962541 A Based on WO 200039189; EP 1141073 A1 Based on WO 200039189; US 2002001720 A1 Div ex US 6294270; US 6423367 B1 Div ex US 6294270

PRAI US 1998-219265 19981223; US 2001-917543 20010727

AB WO 200039189 A UPAB: 20000907

NOVELTY - An electronic circuit device comprises (wt.%) a resin composition containing a curable epoxy-modified aromatic vinyl-conjugated diene block copolymer (1) (90-100), an epoxy resin (0-10) and an epoxy curative. The wt.% of the copolymer and the epoxy resin are based on the epoxy bearing material exclusive of curative.

DETAILED DESCRIPTION - An INDEPENDENT CLAIM is included for a method of using an electronic adhesive, covercoat or encapsulant comprises of incorporating the resin composition as an adhesive, covercoat or encapsulant into an article.

USE - As an electronic adhesive, a covercoat or an encapsulant (claimed) e.g. of adhesive in electronic circuit device includes adherence of a layer of flexible circuitry to another layer of flexible circuitry, to a metal **stiffener**, a semiconductor chip, adherence of copper or other metallic foil to a polymer substrate, adherence of an electronic component such as a semiconductor chip to a circuit on a substrate; adhesives and covercoats in electronic packages; in a **ball grid** arrays (**BGA**), laminated microinterconnects (LMI), chip scale packaging (CSP), chip on board, glass and flexible circuits.

ADVANTAGE - The electronic circuit device exhibits superior solder, heat resistance and moisture insensitivity including the absence of voiding and delamination of the cured resin composition from its substrate. The composition has excellent peel strength and provides over 1000 hours of performance at 85 deg. C. The copolymer resin has excellent resistance to corrosive, aqueous acidic and/or alkaline environments. The partially cured composition shows improved dimensional stability in thermal lamination steps. The device exhibits stability at 85 deg. C and relative humidity 85% for 168 hours followed by a temperature of 220 deg.

C for 10-40 seconds.
Dwg.0/1

L14 ANSWER 5 OF 13 WPIX (C) 2002 THOMSON DERWENT
AN 2000-451583 [39] WPIX
DNN N2000-336224
TI **Ball grid** array semiconductor device package has substrate which includes solder balls which are connected to copper **stiffener** through holes on substrate.
DC U11 V04
IN HASSANZADEH, N; KALIDAS, N; LAMSON, M A
PA (TEXI) TEXAS INSTR INC
CYC 1
PI US 6084777 A 20000704 (200039)* 7p
ADT US 6084777 A Provisional US 1997-44173P 19970423, US 1998-65670 19980423
PRAI US 1997-44173P 19970423; US 1998-65670 19980423
AB US 6084777 A UPAB: 20000818
NOVELTY - Copper **stiffener** (13) is mounted to **heat spreader** (14) provided on substrate (16). Solder balls (20) are formed on the **stiffener** along with holes. A die with several die pads is mounted on the **heat spreader**. The solder balls are connected to the **stiffener** through holes in substrate.
USE - For packing semiconductor devices used in micro electronic mechanical system.
ADVANTAGE - Eliminates the need to form a cavity in a **heat spreader**, thereby overall manufacturing cost is reduced. As **stiffener** can be used as power plane or ground plane, the overall complexity is reduced.
DESCRIPTION OF DRAWING(S) - The figure shows sectional view of **ball grid** array package.
Copper **stiffener** 13
**Heat spreader** 14
Substrate 16
Solder ball 20
Dwg.2/3

L14 ANSWER 6 OF 13 WPIX (C) 2002 THOMSON DERWENT
AN 1999-577126 [49] WPIX
DNN N1999-426283 DNC C1999-168197
TI Fan out type **ball grid** array heat sink structure for semiconductor device - includes **radiation** member foil which **thermally** connects plate on reverse side of insulating tape to electrode of semiconductor device.
DC A85 L03 U11
PA (HITA) HITACHI LTD
CYC 1
PI JP 11251483 A 19990917 (199949)* 12p
ADT JP 11251483 A JP 1998-54715 19980306
PRAI JP 1998-54715 19980306
AB JP 11251483 A UPAB: 19991124
NOVELTY - The reverse side of insulating tape (2) having wiring pattern (3) is provided with a plate (11) which is thermally connected to the electrode (5) of semiconductor device (1) by foil like radiation member (12).
USE - For heat sink type **BGA** for semiconductor device.
ADVANTAGE - Since semiconductor device and **stiffener** are connected with thin flexible heat sink, flexibility of semiconductor

device is secured. Since thin, light weight heat sink is used, fatigue breaking durability of solder becomes longer. Soldering of heat sink to semiconductor device enhance heat release property and versatility.

DESCRIPTION OF DRAWING(S) - The figure shows sectional view of fan-out type **BGA** heat sink structure of semiconductor device.
(1) Semiconductor device; (2) Insulating tape; (3) Wiring pattern; (5) Electrode; (12) Radiation member.
Dwg.1/32

L14 ANSWER 7 OF 13 WPIX (C) 2002 THOMSON DERWENT
AN 1999-276713 [23] WPIX
DNN N1999-207428
TI **Ball grid** array (**BGA**) package comprising dielectric layer with cavity and cutouts, with deformable metal layer coupled to **stiffener** through cutouts.
DC U11
IN HASSANZADEH, N; KALIDAS, N; STEARNS, W P
PA (TEXI) TEXAS INSTR INC
CYC 1
PI US 5895967 A 19990420 (199923)* 12p
ADT US 5895967 A Provisional US 1997-51859P 19970707, US 1998-108552 19980701
PRAI US 1997-51859P 19970707; US 1998-108552 19980701
AB US 5895967 A UPAB: 19991103
NOVELTY - A substrate includes a dielectric layer (10) with a cavity and cutouts. A deformable metal layer includes a cavity, a power ring (26) and a ground ring (24). The deformable metal layer has several portions each partially positioned in one of the cutouts and electrically coupled to a **stiffener** (40) through the cutout.

DETAILED DESCRIPTION - The package (62) includes the substrate, a die (50) and the **stiffener** which has a cavity and is mounted to a **heat spreader** (60). The die is mounted to the **heat spreader** through the cavity in the substrate and the **stiffener**. An INDEPENDENT CLAIM is included for a method for forming a structure using a deformable metal layer.

USE - For high pin count and high frequency devices.

ADVANTAGE - Eliminates multiple substrate layers and the need for expensive metallized vias yet maintains high quality electrical characteristics. Reduces inductance resulting in the electrical benefits of a controlled impedance. Simplifies package fabrication. Enhances signal trace density and signal line routing capability. Reduces overall packaging costs. Improves package reliability by reducing package complexity.

DESCRIPTION OF DRAWING(S) - The drawing shows a perspective view of the **BGA** package.
dielectric layer 10
ground ring 24
power ring 26
**stiffener** 40
die 50
**heat spreader** 60
**BGA** package 62
Dwg.4/8

L14 ANSWER 8 OF 13 WPIX (C) 2002 THOMSON DERWENT
AN 1998-199427 [18] WPIX
DNN N1998-158478
TI **BGA** semiconductor package - includes **stiffener** plate

at which set of slits or pores are provided to absorb and diffuse thermal stress generated in semiconductor chip due to variation in temperature.

DC U11
PA (TOKE) TOSHIBA KK
CYC 1
PI JP 10050877 A 19980220 (199818)* 5p
ADT JP 10050877 A JP 1996-200287 19960730
PRAI JP 1996-200287 19960730
AB JP 10050877 A UPAB: 19980507
The package has a tape carrier (10) which is provided with a conductor pattern. Several electrodes provided along one surface of the tape carrier, are connected with conductor pattern. A semiconductor chip (18) is mounted on the upper surface of the tape carrier. A **stiffener** plate (20) which is used to maintain a flat property of the tape carrier is fixed on the upper surface, so that the semiconductor chip is enclosed.

A rectangular cover plate (30) is attached to the upper surface of the **stiffener** plate so that the cover plate is in contact with the upper surface of the semiconductor chip. A set of slits (26) or pores are provided on the **stiffener** plate to absorb and diffuse thermal stress generated in semiconductor chip due to temperature change.

ADVANTAGE - Absorbs and **disperses thermal** stress generated in semiconductor chip, reliably. Improves reliability of mechanical and electrical connection of semiconductor package.
Dwg.1/7

L14 ANSWER 9 OF 13 WPIX (C) 2002 THOMSON DERWENT
AN 1998-093181 [09] WPIX
DNN N1998-074413
TI **Ball grid** array package type semiconductor device - has **cover** plate which conducts **heat** emitted from chip and is partially bonded to **stiffener** which is used to maintain flat property of TAB tape with solder ball.
DC U11
PA (TOKE) TOSHIBA KK
CYC 1
PI JP 09321085 A 19971212 (199809)* 13p
ADT JP 09321085 A JP 1996-136287 19960530
PRAI JP 1996-136287 19960530
AB JP 09321085 A UPAB: 19980302
The semiconductor device includes a TAB tape (1) which has a solder ball (9). A semiconductor IC chip (5) which uses the solder ball as the exterminal, is bonded to the TAB tape. A **stiffener** (2) is bonded to maintain the flat property of the TAB tape.

A cover plate (7) is provided to conduct heat emitted from the chip. The cover plate is partially bonded to the **stiffener**.

ADVANTAGE - Controls generation of crack resulting from heat on solder ball.
Dwg.1/11

L14 ANSWER 10 OF 13 JAPIO COPYRIGHT 2002 JPO
AN 2001-068512 JAPIO
TI TAB TAPE WITH **STIFFENER** AND **BGA** PACKAGE
IN OTAKA TATSUYA; SUGIMOTO HIROSHI; OMORI TOMOO; SUZUKI YUKIO; TAKAHAGI SHIGEJI; YOSHIOKA OSAMU; ISHII KEIJI
PA HITACHI CABLE LTD
PI JP 2001068512 A 20010316 Heisei
AI JP 1999-241524 (JP11241524 Heisei) 19990827

PRAI JP 1999-241524 19990827
SO PATENT ABSTRACTS OF JAPAN (CD-ROM), Unexamined Applications, Vol. 2001
AB PROBLEM TO BE SOLVED: To provide a TAB tape with a **stiffener**, having good **heat radiating** performance and a **BGA** package.
SOLUTION: This is a TAB tape with a **stiffener**, in which a TAB tape 15 having a wiring pattern 9 is bonded via an adhesive layer 5 to a **stiffener** 2 as a mechanical reinforcing plate and a heat sink. The TAB tape 15 is made by bonding an insulating film 6, such as polyimide film to a copper foil 8 by an adhesive layer 7 or by a baking method, and the first surface of the **stiffener** is covered with a black oxide film 4, and the opposite second surface is covered with a block epoxy resin layer 1, and the **stiffener** is bonded to the TAB tape by the thermosetting adhesive layer 5 having bonding characteristic and reflow characteristic.
COPYRIGHT: (C)2001,JPO

L14 ANSWER 11 OF 13 JAPIO COPYRIGHT 2002 JPO
AN 2000-349203 JAPIO
TI CIRCUIT DEVICE AND MANUFACTURE THEREOF
IN KATO CHIKAYUKI
PA NEC CORP
PI JP 2000349203 A 20001215 Heisei
AI JP 1999-159777 (JP11159777 Heisei) 19990607
PRAI JP 1999-159777 19990607
SO PATENT ABSTRACTS OF JAPAN (CD-ROM), Unexamined Applications, Vol. 2000
AB PROBLEM TO BE SOLVED: To improve productivity and strength of a **BGA**(**ball-grid**-array) package, where a flip chip is mounted on an interposer substrate.
SOLUTION: The gap between the lower surface of a flip chip 2 and the upper surface of an interposer substrate 3 is filled with a single mold resin 101, which is filled with the gap between the upper surface of the interposer substrate 3 and the lower surface of a **heat spreader** 11 as well. The single mold resin 101 is made to contact with a large area at each part for improved joint strength, while it acts as both an underfill resin and a **stiffener** for reduced manufacturing processes and components.
COPYRIGHT: (C)2000,JPO

L14 ANSWER 12 OF 13 JAPIO COPYRIGHT 2002 JPO
AN 1998-261674 JAPIO
TI SEMICONDUCTOR DEVICE AND FABRICATION THEREFOR
IN HATAKEYAMA MAKOTO; OKANE NOBORU; SATO TAKAO; ONO JUNICHI
PA TOSHIBA CORP
PI JP 10261674 A 19980929 Heisei
AI JP 1997-223672 (JP09223672 Heisei) 19970820
PRAI JP 1997-5565 19970116
SO PATENT ABSTRACTS OF JAPAN (CD-ROM), Unexamined Applications, Vol. 1998
AB PROBLEM TO BE SOLVED: To facilitate handling, while enhancing productivity by handling at least one of a package board, a first holder or a second holder as a long body arranged with a plurality of chip-mounting regions, and the like, at constant intervals in the longitudinal direction.
SOLUTION: A long **stiffener** is bonded with a TAB tape piece of good quality by an adhesive. The element-forming face of a chip is covered with an epoxy resin, for example, under a state connected with the TAB tape and is **thermally** set. A **cover** plate piece is bonded onto the long **stiffener** and to the rear side of the chip

by an adhesive. Subsequently, a conductor pad is formed at a ball, connecting position around the chip mounting region on the rear side of the TAB tape, affixed with the **stiffener** and coated with flux before being bonded with a eutectic solder ball. Furthermore, it is heated to activate the flux and to connect the eutectic solder ball with a pad. Finally, it is cut off to obtain a **BGA** package.


L14 ANSWER 13 OF 13 JAPIO COPYRIGHT 2002 JPO
AN 1998-050877 JAPIO
TI SEMICONDUCTOR PACKAGE
IN OGAWA HIDENORI
PA TOSHIBA CORP
PI JP 10050877 A 19980220 Heisei
AI JP 1996-200287 (JP08200287 Heisei) 19960730
PRAI JP 1996-200287 19960730
SO PATENT ABSTRACTS OF JAPAN (CD-ROM), Unexamined Applications, Vol. 1998
AB PROBLEM TO BE SOLVED: To provide a semiconductor package in which reliability of mechanical and electrical connection can be improved by **dispersing** and absorbing occurring **thermal** stress.
SOLUTION: A **BGA** type semiconductor package has a rectangular tape carrier 10. A number of soldering balls 16 are provided on the under face of the tape carrier and a semiconductor chip 18 is mounted on the top face. A rectangular **stiffener** sticks on the top face of the tape carrier so as to surround the semiconductor chip. Further, a rectangular cover plate 30 sticks on the top face of the **stiffener** and on the top face of the semiconductor chip. A plurality of slits 26 for absorbing and **dispersing thermal** stress occurring owing to changes in temperature are opened in corner parts of the **stiffener**.

L17 ANSWER 1 OF 9 WPIX (C) 2002 THOMSON DERWENT
AN 2002-238848 [29] WPIX
CR 2000-038901 [03]
DNN N2002-184114 DNC C2002-071960
TI Circuit chip carrier for integrated circuit die has dielectric adhesive whose coefficient of thermal expansion is higher than that of **stiffener** and flexible dielectric tape.
DC A85 L03 U11
IN HARVEY, P M; PLEPYS, A R
PA (MINN) 3M INNOVATIVE PROPERTIES CO
CYC 1
PI US 2001052647 A1 20011220 (200229)* 15p
ADT US 2001052647 A1 Div ex US 1998-74126 19980507, CIP of US 2000-665030 20000919, US 2001-897182 20010702
FDT US 2001052647 A1 Div ex US 6140707
PRAI US 2001-897182 20010702; US 1998-74126 19980507; US 2000-665030 20000919
AB US2001052647 A UPAB: 20020508
NOVELTY - **Ball grid** array attachment pads (64) and die attachment pads (56) are formed on conductive traces (62) formed on either side of flexible dielectric tape (60). Dielectric adhesive (58) formed on tape (60) has openings for exposing the pads (56). A **stiffener** (52) formed on adhesive has window for exposing the pads (56). Coefficient of thermal expansion of adhesive is higher than that of tape and **stiffener** creating tension in window.
USE - Integrated circuit die such as for tape **ball grid** array (TBGA) package for mounting on **PCB** or any other substrate.
ADVANTAGE - The chip carrier is suitable for anticipating very high flip-chip contact density. Eliminates the need for costly solder mask operation by providing adhesive layer between **stiffener** and tape. Provides very high degree of planarity in the vicinity of the flip-chip connection resulting in improved performance and reliability as thermal expansion coefficient of adhesive is high.
DESCRIPTION OF DRAWING(S) - The figure shows a cross-section of chip carrier.
**Stiffener** 52
Die attachment pads 56
Dielectric adhesive 58
Flexible dielectric tape 60
Conductive traces 62
**Ball grid** array attachment pads 64
Dwg.6/12

L17 ANSWER 2 OF 9 WPIX (C) 2002 THOMSON DERWENT
AN 2002-219068 [28] WPIX
DNN N2002-168068
TI **Ball grid** array package used in high-frequency application, has metallized photovias provided on periphery of circuit traces, and connected to metal **stiffener** and connectable to solder ball.
DC T01 U11 V04 W01 W02 W06
IN OGGIONI, S; VENDRAMIN, G
PA (IBMC) INT BUSINESS MACHINES CORP
CYC 2

PI GB 2358957 A 20010808 (200228)* 14p
TW 457656 A 20011001 (200243)
ADT GB 2358957 A GB 1999-25318 19991027; TW 457656 A TW 2000-108070 20000428
PRAI GB 1999-25318 19991027
AB GB 2358957 A UPAB: 20020502
NOVELTY - Metallized photovias, provided on the periphery of circuit traces, are individually connected to a metal **stiffener** (401) and individually connectable to a solder ball (413). The solder ball is connectable to a mother **board**. The **circuit** traces are provided on a dielectric layer (403) laid on the metal **stiffener**.

USE - Used in high-frequency application e.g. global positioning system application, global system for mobile communications application. For portable digital assistant (PDA) of Bluetooth standard.

ADVANTAGE - Reduces size and thickness of PDA in which module is applied. Improves reliability of package. Does not require drilling operation. Improves electrical performance.

DESCRIPTION OF DRAWING(S) - The figure shows the schematic view of a **ball grid** array package.

Metal **stiffener** 401
Dielectric layer 403
Solder ball 413
Dwg.4/7

L17 ANSWER 3 OF 9 WPIX (C) 2002 THOMSON DERWENT
AN 2001-373310 [39] WPIX
DNN N2001-273007
TI Stress reduction in **BGA PCB** soldering process by adding **stiffener** around or above components e.g. by shielding around **BGA** reduces stress in them.
DC V04 X24
PA (ANON) ANONYMOUS
CYC 1
PI RD 439002 A 20001110 (200139)* 1p
ADT RD 439002 A RD 2000-439002 20001020
PRAI RD 2000-439002 20001020
AB RD 439002 A UPAB: 20010716
NOVELTY - The method involves adding a **stiffener** around or above the components e.g. by shielding around the **BGA** reduces stress in the components. No added parts on the **PCB** modify pads surface without changing pitch just by having elliptical patch. This is obtained for our **PCB** as for **BGA PCB** using CAD electrical, and can improve from 40% the stress level.

USE - In product with **BGA** that are assembled directly on **PCB** by CMS and reflow process.

ADVANTAGE - Cost reduction on line investment, reduction bottleneck, repair-ability, fall off and call rate are reduced.
Dwg.0/0

L17 ANSWER 4 OF 9 WPIX (C) 2002 THOMSON DERWENT
AN 2001-003020 [01] WPIX
DNN N2001-002621
TI Semiconductor package manufacturing method involves mounting semiconductor chip in specific area on substrate and making external terminals to protrude outside mounting area of chip in specific area.
DC U11
PA (SHIH) SEIKO EPSON CORP

CYC 1
PI JP 2000286308 A 20001013 (200101)* 9p
ADT JP 2000286308 A JP 1999-89305 19990330
PRAI JP 1999-89305 19990330
AB JP2000286308 A UPAB: 20001230
NOVELTY - The wiring patterns (20) are formed on substrate (10) including areas (12,14). A semiconductor chip (30) is mounted on area (12). The area (14) is bonded to area (12) in the portion where chip is not mounted so that the areas are connected. The external terminals are protruded outside the mounting area of the chip in area (12).
DETAILED DESCRIPTION - INDEPENDENT CLAIMS are also included for the following:
(a) semiconductor package;
(b) wiring board;
(c) **circuit board**;
(d) electronic device
USE - For manufacturing semiconductor package e.g. tape **ball grid** array (TBGA), chip size package (CSP).
ADVANTAGE - Expensive **stiffener** is not required and size of device is very much reduced.
DESCRIPTION OF DRAWING(S) - The figure shows the explanatory diagram of semiconductor device manufacturing method.
Substrate 10
Areas 12,14
Wiring patterns 20
Semiconductor chip 30
Dwg.2/9

L17 ANSWER 5 OF 9 WPIX (C) 2002 THOMSON DERWENT
AN 2000-531586 [48] WPIX
DNN N2000-393003
TI Electronic packaging assembly has socketing substrate coupled to **motherboard** and embedded with array of electrically conductive pins attached to solder balls.
DC U11 V04
IN KABADI, A N
PA (ITLC) INTEL CORP
CYC 1
PI US 6097609 A 20000801 (200048)* 7p
ADT US 6097609 A US 1998-223647 19981230
PRAI US 1998-223647 19981230
AB US 6097609 A UPAB: 20001001
NOVELTY - The bottom surface of a socketing substrate (335), is aligned horizontally with a **motherboard** (300). An array of electrically conductive pins (340) are embedded through the socketing substrate. The pins have top and bottom ends facing the **motherboard**. The socketing substrate is coupled to the **motherboard** through a series of solder balls (345) which are attached to the bottom of the pins.
DETAILED DESCRIPTION - An electronic component (320) is electrically coupled to the array of pins on the socketing substrate via array of lands (325) on the bottom side of the component. A lid (350) covers the electronic component and wraps around the vertical sides of the socketing substrate.
USE - E.g. **BGA** and LGA package.
ADVANTAGE - Provides a novel design for mounting a **BGA** or LGA component onto board without using a **stiffener**, gold plating or a separate interposer and socketing stage, hence cost is reduced

considerably.
DESCRIPTION OF DRAWING(S) - The figure shows the side view of the assembly applied to a dual sided **motherboard** mounted with electronic components.
**Motherboard** 300
Electronic component 320
Lands 325
Socket substrate 335
Conductive pins 340
Solder balls 345
Lid 350
Dwg.4/4

L17 ANSWER 6 OF 9 WPIX (C) 2002 THOMSON DERWENT
AN 2000-085674 [07] WPIX
DNN N2000-067168 DNC C2000-023903
TI Thermally enhanced tape **ball grid** array package.
DC A85 L03 U11
IN CHIA, C J; LIM, S; LOW, O H
PA (LSIL-N) LSI LOGIC CORP
CYC 1
PI US 6002169 A 19991214 (200007)* 5p
ADT US 6002169 A US 1998-97883 19980615
PRAI US 1998-97883 19980615
AB US 6002169 A UPAB: 20000209
NOVELTY - Holes are arranged in an array pattern through a tape substrate to expose conductive metal traces on the substrate top. A nonconductive **stiffener** frame is attached to the substrate bottom and has through holes corresponding to those in the substrate. An IC mounted on the substrate is electrically connected to the traces. Solder balls are attached to the exposed traces to allow electrical connection of the package to a printed **circuit board** (**PCB**).
DETAILED DESCRIPTION - An INDEPENDENT CLAIM is also included for a **stiffener** frame for use in the package, comprising aluminum that has been anodized to form a protective insulating coating. The **stiffener** frame dissipates heat produced by the IC.
USE - The anodized aluminum frame serves the dual purpose of supporting the tape automated bonding (TAB) substrate during assembly and dissipating heat generated by the IC chip package.
ADVANTAGE - Improved thermal performance, and thus improved device reliability.
DESCRIPTION OF DRAWING(S) - The drawing shows a section of the thermally enhanced tape **ball grid** array package.
traces 115
solder ball pad 117
IC contact pads 123
solder balls 125
substrate holes 130
wire bonding 140
encapsulant 145
**stiffener** frame 155
Dwg.2/3

L17 ANSWER 7 OF 9 WPIX (C) 2002 THOMSON DERWENT
AN 2000-038901 [03] WPIX
DNN N2000-029330 DNC C2000-010028
TI Packaging component for integrated circuit die used in printed

**circuit boards**.
DC A85 G03 L03 U11
IN HARVEY, P M; PLEPYS, A R
PA (MINN) MINNESOTA MINING & MFG CO; (MINN) 3M INNOVATIVE PROPERTIES CO
CYC 24
PI WO 9957764 A1 19991111 (200003)* EN 26p
RW: AT BE CH CY DE DK ES FI FR GB GR IE IT LU MC NL PT SE
W: CA CN JP KR SG
US 6140707 A 20001031 (200057)
EP 1082762 A1 20010314 (200116) EN
R: DE FI FR GB IT NL SE
CN 1302455 A 20010704 (200158)
KR 2001072583 A 20010731 (200209)
ADT WO 9957764 A1 WO 1999-US7087 19990331; US 6140707 A US 1998-74126 19980507; EP 1082762 A1 EP 1999-914308 19990331, WO 1999-US7087 19990331; CN 1302455 A CN 1999-805889 19990331; KR 2001072583 A KR 2000-712348 20001106
FDT EP 1082762 A1 Based on WO 9957764
PRAI US 1998-74126 19980507
AB WO 9957764 A UPAB: 20020508
NOVELTY - The packaging component comprises flexible dielectric tape (60) whose upper surface has selected pattern of conductive traces (62) made of die attachment pads (56) and **ball**- **grid**-array ( **BGA**) attachment pads (64) and lower surface has openings for exposing **BGA** attachment pads. Conductive traces are covered by dielectric adhesive layer (58) attached with **stiffener** (52) having a window.

DETAILED DESCRIPTION - Openings in the adhesive expose die attachment pads.

INDEPENDENT CLAIMS are included for the following: (i) A packaged integrated circuit which has packaging component containing **BGA** solder balls (30) attached to **BGA** attachment pads through the opening and an integrated circuit die (32) disposed within the window formed in the **stiffener**. (ii) Manufacture of packaging component. The **stiffener** is laminated on dielectric adhesive layer using an adhesive. A window is formed in the **stiffener** by etching to expose a portion of the tape and adhesive overlying the die attachment pads. The adhesive overlying die attachment pads are then removed.

USE - The packaging component is used for flip-chip integrated circuit die used in printed **circuit boards**.

ADVANTAGE - The laminated integrated circuit package provides a die attachment site having high degree of planarity arising due to tensile stress in flexible circuit and lamination of adhesive layers on **stiffener**, thereby improving performance and reliability of the circuit. The need for application of high- resolution patterned adhesive and solder mask at the flip-chip attachment site is eliminated since the adhesive layer performs the solder mask function of preventing any bridging between attachment pads.

DESCRIPTION OF DRAWING(S) - The figure illustrates the cross sectional elevational view of integrated circuit and **BGA** solder balls attached to a chip carrier.

**BGA** solder ball 30
Integrated circuit die 32
**Stiffener** 52
Die attachment pad 56
Dielectric adhesive layer 58

Flexible dielectric tape 60
Conductive trace 62
**BGA** attachment pad 64
Dwg.6/8

L17 ANSWER 8 OF 9 WPIX (C) 2002 THOMSON DERWENT
AN 2000-005225 [01] WPIX
CR 1996-012637 [02]; 1999-266092 [23]; 2002-342601 [38]
DNN N2000-004668
TI Heat resistive structure for **ball grid** array, land grid array type semiconductor device - has **stiffener** placed between printed **circuit board** mounted with semiconductor device and metal plate located on top of semiconductor device.
DC U11 V04
IN AKAI, T; HAMANO, T; IIJIMA, M; MINAMIZAWA, M; MIZUKOSHI, M; NUKIWA, M; TAKENAKA, M; WAKABAYASHI, T; YAMASHITA, T
PA (FUIT) FUJITSU LTD; (AKAI-I) AKAI T; (HAMA-I) HAMANO T; (IIJI-I) IIJIMA M; (MINA-I) MINAMIZAWA M; (MIZU-I) MIZUKOSHI M; (NUKI-I) NUKIWA M; (TAKE-I) TAKENAKA M; (WAKA-I) WAKABAYASHI T; (YAMA-I) YAMASHITA T
CYC 2
PI JP 11284097 A 19991015 (200001)* 9p
US 2002001178 A1 20020103 (200207)
US 6347037 B2 20020212 (200219)
ADT JP 11284097 A JP 1998-83882 19980330; US 2002001178 A1 Cont of US 1995-423632 19950417, Div ex US 1997-782381 19970113, CIP of US 1997-924958 19970908, US 1998-185716 19981104; US 6347037 B2 Cont of US 1995-423632 19950417, Div ex US 1997-782381 19970113, CIP of US 1997-924958 19970908, US 1998-185716 19981104
FDT US 2002001178 A1 Div ex US 5729435, CIP of US 5978222; US 6347037 B2 Div ex US 5729435
PRAI JP 1998-83882 19980330; JP 1994-92155 19940428; JP 1995-59562 19950317
AB JP 11284097 A UPAB: 20020618
NOVELTY - Semiconductor device (14) is mounted on printed **circuit board** (**PCB**)(12) by adhesive (24) and metal plate (18) is fixed over the device. A **stiffener** (16) bonded between **PCB** and metal plate by adhesive (26), has central recess (30) for housing the device. The material for **stiffener**, metal plate and **PCB** are selected such that their thermal expansion coefficient satisfy specific relation.
USE - For preventing thermal deformation in **ball grid** array, land grid array type semiconductor device.
ADVANTAGE - As **stiffener** is placed between **PCB** and metal plate, stress due to different thermal expansion coefficient of material is prevented. Crack in junctions in the device does not take place and reliability is improved. DESCRIPTION OF DRAWING(S) - The figure shows the sectional view of semiconductor enclosing arrangement. (12) Printed **circuit board**; (14) Semiconductor device; (16) **Stiffener**; (18) metal plate; (24,26) Adhesives; (30) Central recess.
Dwg.1/3

L17 ANSWER 9 OF 9 WPIX (C) 2002 THOMSON DERWENT
AN 1999-504502 [42] WPIX
DNN N1999-377310
TI Potential measurement **circuit** for **circuit**

**board** in PGA package, IC package - has several through-holes configured from cover plate to current carrying section of **circuit board** through **stiffener**.

DC S01 U11
PA (TOKE) TOSHIBA KK
CYC 1
PI JP 11220057 A 19990810 (199942)* 8p
ADT JP 11220057 A JP 1998-19673 19980130
PRAI JP 1998-19673 19980130
AB JP 11220057 A UPAB: 19991026

NOVELTY - Semiconductor chip (16) is mounted in rear side of solder ball (15). A **stiffener** (19) is used to fix **circuit board**. A cover plate (21) is bonded on surface of both chip and **stiffener**, using an adhesive agent (20). Resin sealing (17) is provided for chip. Several through-holes (22,23) are provided to the current-carrying sections of **circuit board** through **stiffener** from cover plate. DETAILED DESCRIPTION - An INDEPENDENT CLAIM is also included for the temperature measurement method of semiconductor chip in PGA package.

USE - For measuring potential of arbitrary points on **circuit board** connected to semiconductor chip in PGA package, IC chip.

ADVANTAGE - Several terminals for a test can be provided without using a signal pin. DESCRIPTION OF DRAWING(S) - The figure shows the structural drawing of **ball grid** array package. (15) Solder ball; (16) Semiconductor chip; (17) Resin; (19) **Stiffener** ; (20) Adhesive agent; (21) Cover plate; (22,23) Through-holes. Dwg.1/8

L17 ANSWER 1 OF 9 WPIX (C) 2002 THOMSON DERWENT
AN 2002-238848 [29] WPIX
CR 2000-038901 [03]
DNN N2002-184114 DNC C2002-071960
TI Circuit chip carrier for integrated circuit die has dielectric adhesive whose coefficient of thermal expansion is higher than that of **stiffener** and flexible dielectric tape.
DC A85 L03 U11
IN HARVEY, P M; PLEPYS, A R
PA (MINN) 3M INNOVATIVE PROPERTIES CO
CYC 1
PI US 2001052647 A1 20011220 (200229)* 15p
ADT US 2001052647 A1 Div ex US 1998-74126 19980507, CIP of US 2000-665030 20000919, US 2001-897182 20010702
FDT US 2001052647 A1 Div ex US 6140707
PRAI US 2001-897182 20010702; US 1998-74126 19980507; US 2000-665030 20000919
AB US2001052647 A UPAB: 20020508
NOVELTY - **Ball grid** array attachment pads (64) and die attachment pads (56) are formed on conductive traces (62) formed on either side of flexible dielectric tape (60). Dielectric adhesive (58) formed on tape (60) has openings for exposing the pads (56). A **stiffener** (52) formed on adhesive has window for exposing the pads (56). Coefficient of thermal expansion of adhesive is higher than that of tape and **stiffener** creating tension in window.
USE - Integrated circuit die such as for tape **ball grid** array (TBGA) package for mounting on **PCB** or any other substrate.
ADVANTAGE - The chip carrier is suitable for anticipating very high flip-chip contact density. Eliminates the need for costly solder mask operation by providing adhesive layer between **stiffener** and tape. Provides very high degree of planarity in the vicinity of the flip-chip connection resulting in improved performance and reliability as thermal expansion coefficient of adhesive is high.
DESCRIPTION OF DRAWING(S) - The figure shows a cross-section of chip carrier.
**Stiffener** 52
Die attachment pads 56
Dielectric adhesive 58
Flexible dielectric tape 60
Conductive traces 62
**Ball grid** array attachment pads 64
Dwg.6/12

L17 ANSWER 2 OF 9 WPIX (C) 2002 THOMSON DERWENT
AN 2002-219068 [28] WPIX
DNN N2002-168068
TI **Ball grid** array package used in high-frequency application, has metallized photovias provided on periphery of circuit traces, and connected to metal **stiffener** and connectable to solder ball.
DC T01 U11 V04 W01 W02 W06
IN OGGIONI, S; VENDRAMIN, G
PA (IBMC) INT BUSINESS MACHINES CORP
CYC 2

PI GB 2358957 A 20010808 (200228)* 14p
TW 457656 A 20011001 (200243)
ADT GB 2358957 A GB 1999-25318 19991027; TW 457656 A TW 2000-108070 20000428
PRAI GB 1999-25318 19991027
AB GB 2358957 A UPAB: 20020502
NOVELTY - Metallized photovias, provided on the periphery of circuit traces, are individually connected to a metal **stiffener** (401) and individually connectable to a solder ball (413). The solder ball is connectable to a mother **board**. The **circuit** traces are provided on a dielectric layer (403) laid on the metal **stiffener**.

USE - Used in high-frequency application e.g. global positioning system application, global system for mobile communications application. For portable digital assistant (PDA) of Bluetooth standard.

ADVANTAGE - Reduces size and thickness of PDA in which module is applied. Improves reliability of package. Does not require drilling operation. Improves electrical performance.

DESCRIPTION OF DRAWING(S) - The figure shows the schematic view of a **ball grid** array package.

Metal **stiffener** 401
Dielectric layer 403
Solder ball 413
Dwg.4/7

L17 ANSWER 3 OF 9 WPIX (C) 2002 THOMSON DERWENT
AN 2001-373310 [39] WPIX
DNN N2001-273007
TI Stress reduction in **BGA PCB** soldering process by adding **stiffener** around or above components e.g. by shielding around **BGA** reduces stress in them.
DC V04 X24
PA (ANON) ANONYMOUS
CYC 1
PI RD 439002 A 20001110 (200139)* 1p
ADT RD 439002 A RD 2000-439002 20001020
PRAI RD 2000-439002 20001020
AB RD 439002 A UPAB: 20010716
NOVELTY - The method involves adding a **stiffener** around or above the components e.g. by shielding around the **BGA** reduces stress in the components. No added parts on the **PCB** modify pads surface without changing pitch just by having elliptical patch. This is obtained for our **PCB** as for **BGA PCB** using CAD electrical, and can improve from 40% the stress level.

USE - In product with **BGA** that are assembled directly on **PCB** by CMS and reflow process.

ADVANTAGE - Cost reduction on line investment, reduction bottleneck, repair-ability, fall off and call rate are reduced.
Dwg.0/0

L17 ANSWER 4 OF 9 WPIX (C) 2002 THOMSON DERWENT
AN 2001-003020 [01] WPIX
DNN N2001-002621
TI Semiconductor package manufacturing method involves mounting semiconductor chip in specific area on substrate and making external terminals to protrude outside mounting area of chip in specific area.
DC U11
PA (SHIH) SEIKO EPSON CORP

CYC 1
PI JP 2000286308 A 20001013 (200101)* 9p
ADT JP 2000286308 A JP 1999-89305 19990330
PRAI JP 1999-89305 19990330
AB JP2000286308 A UPAB: 20001230
NOVELTY - The wiring patterns (20) are formed on substrate (10) including areas (12,14). A semiconductor chip (30) is mounted on area (12). The area (14) is bonded to area (12) in the portion where chip is not mounted so that the areas are connected. The external terminals are protruded outside the mounting area of the chip in area (12).
DETAILED DESCRIPTION - INDEPENDENT CLAIMS are also included for the following:
(a) semiconductor package;
(b) wiring board;
(c) **circuit board**;
(d) electronic device
USE - For manufacturing semiconductor package e.g. tape **ball grid** array (TBGA), chip size package (CSP).
ADVANTAGE - Expensive **stiffener** is not required and size of device is very much reduced.
DESCRIPTION OF DRAWING(S) - The figure shows the explanatory diagram of semiconductor device manufacturing method.
Substrate 10
Areas 12,14
Wiring patterns 20
Semiconductor chip 30
Dwg.2/9

L17 ANSWER 5 OF 9 WPIX (C) 2002 THOMSON DERWENT
AN 2000-531586 [48] WPIX
DNN N2000-393003
TI Electronic packaging assembly has socketing substrate coupled to **motherboard** and embedded with array of electrically conductive pins attached to solder balls.
DC U11 V04
IN KABADI, A N
PA (ITLC) INTEL CORP
CYC 1
PI US 6097609 A 20000801 (200048)* 7p
ADT US 6097609 A US 1998-223647 19981230
PRAI US 1998-223647 19981230
AB US 6097609 A UPAB: 20001001
NOVELTY - The bottom surface of a socketing substrate (335), is aligned horizontally with a **motherboard** (300). An array of electrically conductive pins (340) are embedded through the socketing substrate. The pins have top and bottom ends facing the **motherboard**. The socketing substrate is coupled to the **motherboard** through a series of solder balls (345) which are attached to the bottom of the pins.
DETAILED DESCRIPTION - An electronic component (320) is electrically coupled to the array of pins on the socketing substrate via array of lands (325) on the bottom side of the component. A lid (350) covers the electronic component and wraps around the vertical sides of the socketing substrate.
USE - E.g. **BGA** and LGA package.
ADVANTAGE - Provides a novel design for mounting a **BGA** or LGA component onto board without using a **stiffener**, gold plating or a separate interposer and socketing stage, hence cost is reduced

considerably.
DESCRIPTION OF DRAWING(S) - The figure shows the side view of the assembly applied to a dual sided **motherboard** mounted with electronic components.
**Motherboard** 300
Electronic component 320
Lands 325
Socket substrate 335
Conductive pins 340
Solder balls 345
Lid 350
Dwg.4/4

L17 ANSWER 6 OF 9 WPIX (C) 2002 THOMSON DERWENT
AN 2000-085674 [07] WPIX
DNN N2000-067168 DNC C2000-023903
TI Thermally enhanced tape **ball grid** array package.
DC A85 L03 U11
IN CHIA, C J; LIM, S; LOW, O H
PA (LSIL-N) LSI LOGIC CORP
CYC 1
PI US 6002169 A 19991214 (200007)* 5p
ADT US 6002169 A US 1998-97883 19980615
PRAI US 1998-97883 19980615
AB US 6002169 A UPAB: 20000209
NOVELTY - Holes are arranged in an array pattern through a tape substrate to expose conductive metal traces on the substrate top. A nonconductive **stiffener** frame is attached to the substrate bottom and has through holes corresponding to those in the substrate. An IC mounted on the substrate is electrically connected to the traces. Solder balls are attached to the exposed traces to allow electrical connection of the package to a printed **circuit board** (**PCB**).
DETAILED DESCRIPTION - An INDEPENDENT CLAIM is also included for a **stiffener** frame for use in the package, comprising aluminum that has been anodized to form a protective insulating coating. The **stiffener** frame dissipates heat produced by the IC.
USE - The anodized aluminum frame serves the dual purpose of supporting the tape automated bonding (TAB) substrate during assembly and dissipating heat generated by the IC chip package.
ADVANTAGE - Improved thermal performance, and thus improved device reliability.
DESCRIPTION OF DRAWING(S) - The drawing shows a section of the thermally enhanced tape **ball grid** array package.
traces 115
solder ball pad 117
IC contact pads 123
solder balls 125
substrate holes 130
wire bonding 140
encapsulant 145
**stiffener** frame 155
Dwg.2/3

L17 ANSWER 7 OF 9 WPIX (C) 2002 THOMSON DERWENT
AN 2000-038901 [03] WPIX
DNN N2000-029330 DNC C2000-010028
TI Packaging component for integrated circuit die used in printed

**circuit boards**.
DC A85 G03 L03 U11
IN HARVEY, P M; PLEPYS, A R
PA (MINN) MINNESOTA MINING & MFG CO; (MINN) 3M INNOVATIVE PROPERTIES CO
CYC 24
PI WO 9957764 A1 19991111 (200003)* EN 26p
RW: AT BE CH CY DE DK ES FI FR GB GR IE IT LU MC NL PT SE
W: CA CN JP KR SG
US 6140707 A 20001031 (200057)
EP 1082762 A1 20010314 (200116) EN
R: DE FI FR GB IT NL SE
CN 1302455 A 20010704 (200158)
KR 2001072583 A 20010731 (200209)
ADT WO 9957764 A1 WO 1999-US7087 19990331; US 6140707 A US 1998-74126 19980507; EP 1082762 A1 EP 1999-914308 19990331, WO 1999-US7087 19990331; CN 1302455 A CN 1999-805889 19990331; KR 2001072583 A KR 2000-712348 20001106
FDT EP 1082762 A1 Based on WO 9957764
PRAI US 1998-74126 19980507
AB WO 9957764 A UPAB: 20020508
NOVELTY - The packaging component comprises flexible dielectric tape (60) whose upper surface has selected pattern of conductive traces (62) made of die attachment pads (56) and **ball**- **grid**-array ( **BGA**) attachment pads (64) and lower surface has openings for exposing **BGA** attachment pads. Conductive traces are covered by dielectric adhesive layer (58) attached with **stiffener** (52) having a window.

DETAILED DESCRIPTION - Openings in the adhesive expose die attachment pads.

INDEPENDENT CLAIMS are included for the following: (i) A packaged integrated circuit which has packaging component containing **BGA** solder balls (30) attached to **BGA** attachment pads through the opening and an integrated circuit die (32) disposed within the window formed in the **stiffener**. (ii) Manufacture of packaging component. The **stiffener** is laminated on dielectric adhesive layer using an adhesive. A window is formed in the **stiffener** by etching to expose a portion of the tape and adhesive overlying the die attachment pads. The adhesive overlying die attachment pads are then removed.

USE - The packaging component is used for flip-chip integrated circuit die used in printed **circuit boards**.

ADVANTAGE - The laminated integrated circuit package provides a die attachment site having high degree of planarity arising due to tensile stress in flexible circuit and lamination of adhesive layers on **stiffener**, thereby improving performance and reliability of the circuit. The need for application of high- resolution patterned adhesive and solder mask at the flip-chip attachment site is eliminated since the adhesive layer performs the solder mask function of preventing any bridging between attachment pads.

DESCRIPTION OF DRAWING(S) - The figure illustrates the cross sectional elevational view of integrated circuit and **BGA** solder balls attached to a chip carrier.

**BGA** solder ball 30
Integrated circuit die 32
**Stiffener** 52
Die attachment pad 56
Dielectric adhesive layer 58

Flexible dielectric tape 60
Conductive trace 62
**BGA** attachment pad 64
Dwg.6/8

L17 ANSWER 8 OF 9 WPIX (C) 2002 THOMSON DERWENT
AN 2000-005225 [01] WPIX
CR 1996-012637 [02]; 1999-266092 [23]; 2002-342601 [38]
DNN N2000-004668
TI Heat resistive structure for **ball grid** array, land grid array type semiconductor device - has **stiffener** placed between printed **circuit board** mounted with semiconductor device and metal plate located on top of semiconductor device.
DC U11 V04
IN AKAI, T; HAMANO, T; IIJIMA, M; MINAMIZAWA, M; MIZUKOSHI, M; NUKIWA, M; TAKENAKA, M; WAKABAYASHI, T; YAMASHITA, T
PA (FUIT) FUJITSU LTD; (AKAI-I) AKAI T; (HAMA-I) HAMANO T; (IIJI-I) IIJIMA M; (MINA-I) MINAMIZAWA M; (MIZU-I) MIZUKOSHI M; (NUKI-I) NUKIWA M; (TAKE-I) TAKENAKA M; (WAKA-I) WAKABAYASHI T; (YAMA-I) YAMASHITA T
CYC 2
PI JP 11284097 A 19991015 (200001)* 9p
US 2002001178 A1 20020103 (200207)
US 6347037 B2 20020212 (200219)
ADT JP 11284097 A JP 1998-83882 19980330; US 2002001178 A1 Cont of US 1995-423632 19950417, Div ex US 1997-782381 19970113, CIP of US 1997-924958 19970908, US 1998-185716 19981104; US 6347037 B2 Cont of US 1995-423632 19950417, Div ex US 1997-782381 19970113, CIP of US 1997-924958 19970908, US 1998-185716 19981104
FDT US 2002001178 A1 Div ex US 5729435, CIP of US 5978222; US 6347037 B2 Div ex US 5729435
PRAI JP 1998-83882 19980330; JP 1994-92155 19940428; JP 1995-59562 19950317
AB JP 11284097 A UPAB: 20020618
NOVELTY - Semiconductor device (14) is mounted on printed **circuit board** (**PCB**)(12) by adhesive (24) and metal plate (18) is fixed over the device. A **stiffener** (16) bonded between **PCB** and metal plate by adhesive (26), has central recess (30) for housing the device. The material for **stiffener**, metal plate and **PCB** are selected such that their thermal expansion coefficient satisfy specific relation.
USE - For preventing thermal deformation in **ball grid** array, land grid array type semiconductor device.
ADVANTAGE - As **stiffener** is placed between **PCB** and metal plate, stress due to different thermal expansion coefficient of material is prevented. Crack in junctions in the device does not take place and reliability is improved. DESCRIPTION OF DRAWING(S) - The figure shows the sectional view of semiconductor enclosing arrangement. (12) Printed **circuit board**; (14) Semiconductor device; (16) **Stiffener**; (18) metal plate; (24,26) Adhesives; (30) Central recess.
Dwg.1/3

L17 ANSWER 9 OF 9 WPIX (C) 2002 THOMSON DERWENT
AN 1999-504502 [42] WPIX
DNN N1999-377310
TI Potential measurement **circuit** for **circuit**

**board** in PGA package, IC package - has several through-holes configured from cover plate to current carrying section of **circuit board** through **stiffener**.

DC S01 U11
PA (TOKE) TOSHIBA KK
CYC 1
PI JP 11220057 A 19990810 (199942)* 8p
ADT JP 11220057 A JP 1998-19673 19980130
PRAI JP 1998-19673 19980130
AB JP 11220057 A UPAB: 19991026

NOVELTY - Semiconductor chip (16) is mounted in rear side of solder ball (15). A **stiffener** (19) is used to fix **circuit board**. A cover plate (21) is bonded on surface of both chip and **stiffener**, using an adhesive agent (20). Resin sealing (17) is provided for chip. Several through-holes (22,23) are provided to the current-carrying sections of **circuit board** through **stiffener** from cover plate. DETAILED DESCRIPTION - An INDEPENDENT CLAIM is also included for the temperature measurement method of semiconductor chip in PGA package.

USE - For measuring potential of arbitrary points on **circuit board** connected to semiconductor chip in PGA package, IC chip.

ADVANTAGE - Several terminals for a test can be provided without using a signal pin. DESCRIPTION OF DRAWING(S) - The figure shows the structural drawing of **ball grid** array package. (15) Solder ball; (16) Semiconductor chip; (17) Resin; (19) **Stiffener**; (20) Adhesive agent; (21) Cover plate; (22,23) Through-holes.

Dwg.1/8

L20 ANSWER 1 OF 21 WPIX (C) 2002 THOMSON DERWENT
AN 2002-499268 [53] WPIX
CR 1998-610652 [51]
DNN N2002-395265
TI Package for semiconductor chip, has **solder ball** filling the path defined by through-hole in flex tape interconnect substrate.
DC U11 V04
IN RYU, S R; SOHN, J Y
PA (SIGN-N) SIGNETICS KP CO LTD
CYC 1
PI US 2002050407 A1 20020502 (200253)* 31p
ADT US 2002050407 A1 CIP of US 1997-892471 19970714, Cont of US 1999-422212 19991019, US 2001-13177 20011207
PRAI US 1999-422212 19991019; US 1997-892471 19970714; US 2001-13177 20011207
AB US2002050407 A UPAB: 20020820
NOVELTY - A flex tape interconnect substrate (150) attached to the ground plane (160), has a through-hole (119) defining a path to the ground plane. A **solder ball** (120a) contacting with the ground plane fills the path defined by the through-hole.
USE - E.g. tape **ball grid** array (TBGA) semiconductor device packages for mounting integrated circuit.
ADVANTAGE - Provides TBGA packages with improved heat dissipation, lower electrical noise and improved density. The TBGA package is thinner, lighter and less expensive. Provides efficient manufacturing of semiconductor packages that increase yield, provides high performance and reduces manufacturing cost.
DESCRIPTION OF DRAWING(S) - The figure shows a cross-sectional view of **ball grid** array package having a **heat spreader**, a ground plane and a single **metal** layer flex tape interconnect substrate wire bonded to the semiconductor die.
Through-hole 119
**Solder ball** 120a
Flex tape interconnect substrate 150
Ground plane 160
Dwg.3A/7

L20 ANSWER 2 OF 21 WPIX (C) 2002 THOMSON DERWENT
AN 2002-163107 [21] WPIX
DNN N2002-124466 DNC C2002-050281
TI Low-profile semiconductor device, e.g. **ball grid** array device, includes second encapsulant formed to encapsulate **solder balls** or lumps with bottom ends exposed to and flush with bottom surface of second encapsulant.
DC L03 U11
IN BAI, J; TSAI, C
PA (UNTE-N) UNITED TEST CENT INC
CYC 27
PI US 6326700 B1 20011204 (200221)* 11p
EP 1205973 A1 20020515 (200239)# EN

R: AL AT BE CH CY DE DK ES FI FR GB GR IE IT LI LT LU LV MC MK NL PT RO SE SI TR

ADT US 6326700 B1 US 2000-639202 20000815; EP 1205973 A1 EP 2000-124579 20001110

PRAI US 2000-639202 20000815; EP 2000-124579 20001110

AB US 6326700 B UPAB: 20020403

NOVELTY - A low-profile semiconductor device has a substrate, a semiconductor die, gold wires and **solder balls** or lumps, and two encapsulants. The second encapsulant is formed over the conductive traces of the substrate to encapsulate the conductive traces, gold wires, a hole, and **solder balls** or lumps with bottom ends exposed to or flush with a bottom surface of the second encapsulant.

DETAILED DESCRIPTION - A low-profile semiconductor device comprises a substrate (41), a semiconductor die (40), gold wires and **solder balls** or lumps, and two encapsulants. The substrate has a base layer and conductive traces formed on the base layer. The base layer is formed with at least a hole. The semiconductor die has an active surface and an opposing inactive surface. It is mounted on the base layer of the substrate via the active surface. The gold wires pass through the hole in the substrate for electrically coupling the semiconductor die to the conductive traces on the substrate. The **solder balls** or lumps are arranged on terminals of the conductive traces for electrically connecting the semiconductor die to external devices. The first encapsulant is formed on the substrate to encapsulate the semiconductor die. The second encapsulant is formed over the conductive traces of the substrate to encapsulate the conductive traces, the gold wires, and the hole. It is also formed to encapsulate **solder balls** or lumps with bottom ends exposed to and flush with the bottom surface of the second encapsulant. An INDEPENDENT CLAIM is also included for a method of manufacturing a low-profile semiconductor device.

USE - As low-profile semiconductor device, e.g. **ball grid** array devices.

ADVANTAGE - The device has a reduced overall thickness. It eliminates warpage of the device such that the occurrence of delamination between the semiconductor die and the substrate can be effectively prevented. It can improve the accuracy of testing of electrical performance. It can be electrically connected to an external device in a quality-assured way than the prior art. The substrate of the device needs not to be coated with solder mask, thus reducing the cost for making the substrate.

DESCRIPTION OF DRAWING(S) - The figure is a cross-sectional view of a semiconductor device.

semiconductor die 40

substrate 41

upper encapsulant 43

**heat spreader** 46

top surface 430

Dwg.6/11

L20 ANSWER 3 OF 21 WPIX (C) 2002 THOMSON DERWENT

AN 2001-594528 [67] WPIX

TI **Ball grid** array-typed substrate assembly and semiconductor package.

DC U11

IN AHN, J S; KIM, Y Y; RYU, J C

PA (SMSU) SAMSUNG TECHWIN CO LTD

CYC 1

PI KR 2001038773 A 20010515 (200167)* 1p
ADT KR 2001038773 A KR 1999-46889 19991027
PRAI KR 1999-46889 19991027
AB KR2001038773 A UPAB: 20011119
NOVELTY - **Ball grid** array-typed substrate assembly and a semiconductor package are to easily **radiate** the **heat** produced from a semiconductor chip by forming sink on the package.
DETAILED DESCRIPTION - A number of openings(21a) are formed on a substrate. A wire pad(22) is provided at a desired spacing on an edge of the opening, and one end of a wire(23) is bonded on the wire pad. At least one dam ring(24) is provided on the substrate(21), with the dam ring forming a band along the edge of the opening. A number of **solder balls** are attached to an outer surface of the dam ring. The substrate is attached with a semiconductor chip(27) on a bottom thereof, and the other end of the wire is connected to the semiconductor chip through the opening. The semiconductor chip is attached with a heat sink(29) by an adhesive. The heat sink is made of a **metal** material to efficiently **radiate** the **heat** produced from the semiconductor chip. The dam ring is provided on an inner surface with a sealant(25) to protect a bonded portion of an exposed upper surface of the semiconductor chip from the exterior.
Dwg.1/10

L20 ANSWER 4 OF 21 WPIX (C) 2002 THOMSON DERWENT
AN 2001-212757 [22] WPIX
DNN N2001-151982 DNC C2001-063592
TI Integrated circuit **ball grid** array package, has conductive layers at ground potential formed on opposite sides of signal and power lines to lower self and mutual inductances.
DC A85 L03 U11 V04
IN JAMES, R D; LAMSON, M A
PA (TEXI) TEXAS INSTR INC
CYC 26
PI EP 1079433 A2 20010228 (200122)* EN 9p
R: AL AT BE CH CY DE DK ES FI FR GB GR IE IT LI LT LU LV MC MK NL PT RO SE SI
JP 2002076179 A 20020315 (200234)# 8p
ADT EP 1079433 A2 EP 2000-117329 20000821; JP 2002076179 A JP 2000-255641 20000825
PRAI US 1999-151016P 19990827; JP 2000-255641 20000825
AB EP 1079433 A UPAB: 20010421
NOVELTY - High performance integrated circuit (IC) package comprises:
(a) a first conductive layer (115) providing ground potential; and
(b) a second conductive layer (105) also at ground potential.
The conductive layers are formed on opposite sides of signal and power lines so that self and mutual inductances are lowered, to reduce package electrical noise and cross-talk, and increase circuit switching and speed.
DETAILED DESCRIPTION - An INDEPENDENT CLAIM is also included for a method of fabricating a high performance, high I/O **ball grid** array (**BGA**) package, which comprises:
(i) providing a substrate (110) having two **metal** layers (115, 116) and an intermediate insulating layer (113) having **metal** filled vias (114) in it;
(ii) forming the **metal** layers such that one (115) provides electrical ground potential, and the other (116) provides electrical signal and power potentials;

(iii) forming protective insulating films (111, 112), usable as solder masks, over the exposed surfaces of the **metal** layers, of a thickness which reduces electrical inductances of the signal and power lines;

(iv) forming openings (123, 112a) in both insulating films, and filling them with solderable **metal** to create attachment sites for outside **solder balls** and chip **solder** bumps;

(v) attaching an IC chip (101), having an active surface (101a) including solder bumps (102) and a passive surface (101b), by adhering the solder bumps to the **metal** filled openings in one of the insulating films (111);

(vi) attaching part of a **heat spreader** to the passive surface;

(vii) attaching the remaining parts of the **heat spreader** to the insulating film (111) using an electrically conductive adhesive (130); and

(viii) attaching **solder balls** (106) to the **metal** filled openings (112a) in the other insulating film (112).

USE - For high performance **BGA** packages for flip chip assembly.

ADVANTAGE - Package electrical noise and cross-talk are reduced, and IC switching and speed are increased.

DESCRIPTION OF DRAWING(S) - The drawing shows a cross-section through the above **BGA** package.

IC chip 101
active surface 101a
passive surface 101b
solder bumps 102
second conductive layer 105
**solder balls** 106
first and second insulating layers 111, 112
intermediate insulating layer 113
**metal** filled vias 114
first conductive layer 115
**metal** layer 116
openings 123, 112a
conductive adhesive 130

Dwg.1/4

L20 ANSWER 5 OF 21 WPIX (C) 2002 THOMSON DERWENT
AN 2000-364290 [31] WPIX
DNN N2000-272620 DNC C2000-109842
TI Integrated circuit package e.g. **ball grid** array package has flex tape which has conductive **metal** lead pattern positioned on side of tape facing substrate with apertures, exposes lead pattern for **solder ball** bonding.
DC A85 L03 U11
IN ALAGARATNAM, M; CHIA, C J; LOW, Q H
PA (LSIL-N) LSI LOGIC CORP
CYC 1
PI US 6057594 A 20000502 (200031)* 5p
ADT US 6057594 A US 1997-842379 19970423
PRAI US 1997-842379 19970423
AB US 6057594 A UPAB: 20000630
NOVELTY - IC package has molded plastic base structure sandwiched between heat conductive substrate (4) and flex tape (16). Flex tape has conductive

**metal** lead pattern (18) positioned on tape side facing substrate with apertures (22) that exposes lead pattern for **solder ball** bonding. Semiconductor IC (12) is mounted on central point of **heat spreader** (10). Chip and wiring bonding are then encapsulated on substrate.

DETAILED DESCRIPTION - A molded plastic base structure includes heat conductive substrate and flex tape extending from corresponding side of substrate. The heat conductive substrate is laminate structure comprising **metal** and ceramics. The molded plastic material is present between substrate and flex tape which has conductive **metal** lead pattern on the tape side which faces the substrate. Apertures exposes conductive lead pattern for **solder ball** bonding. A semiconductor IC chip with active and non-active side is mounted to central portion of **heat spreader** and active side has bond pads (14) for interconnecting integrated circuit. Wire bonding interconnects bond pads on clip to **metal** lead pattern chip. The wire bonding are then encapsulated on substrate by filling cavity in the substrate partially by a resin. The cavity has molded plastic along its side walls. The flex tape also extends along side walls of cavity.

USE - For large scale integrated (LSI) circuits, integrated circuit (IC) packages e.g. **ball grid** array (**BGA**) package, formed by tape automated bonding (TAB).

ADVANTAGE - As chip is directly fixed to **heat spreader heat** dissipation is increased. Wire bonding is lower in cost and has flexibility higher then tape automated bonding (TAB) hence resulting package is economical to manufacture, thin and light weight.

DESCRIPTION OF DRAWING(S) - The figure shows perspective view of **ball grid** array package.

Heat conductive substrate 4

**Heat spreader** 10

Semiconductor integrated chip 12

Bond pads 14

Flex tape 16

lead pattern 18

Apertures 22

Dwg.3/5

L20 ANSWER 6 OF 21 WPIX (C) 2002 THOMSON DERWENT
AN 1998-597117 [51] WPIX
DNN N1998-464724 DNC C1998-179352
TI Thin power tape **ball grid** array package - has semiconductor chip mounted in **heat spreader** recess and its bonding pads connected to **metal** interconnect patterns on flex tape..
DC A85 L03 U11
IN ALAGARATNAM, M; CHIA, C J; VARIOT, P
PA (LSIL-N) LSI LOGIC CORP
CYC 27
PI EP 880175 A2 19981125 (199851)* EN 5p
R: AL AT BE CH CY DE DK ES FI FR GB GR IE IT LI LT LU LV MC MK NL PT RO SE SI
JP 11003957 A 19990106 (199911) 4p
US 5869889 A 19990209 (199913)
ADT EP 880175 A2 EP 1998-303039 19980421; JP 11003957 A JP 1998-109632 19980420; US 5869889 A US 1997-840614 19970421
PRAI US 1997-840614 19970421

AB EP 880175 A UPAB: 19981223
Package comprises a heat conductive support (10) formed to have a recessed portion with opposing planar surfaces (12,14) and a centrally disposed surface (16). Flex tape is attached to the planar surfaces (12,14) and extends to the centrally disposed surface (16). The flex tape includes one or more **metal** interconnect patterns (22) on an exposed surface. Semiconductor integrated circuit chip (24) is mounted on centrally disposed surface (16) spaced from the flex tape (18,20). Chip (24) has bonding pads (26). Wire bonds interconnect pads (26) to the interconnect pattern (22). Preferably chip (24) and the wire bonds are encapsulated by plastic molding or epoxy on the heat conductive support (10). Preferably the **metal** interconnect pattern (22) is connected by **solder balls** to a mother board.
USE - Flex tape **ball grid** array package where the flex tape and a formed **heat spreader** provide the package substrate.
ADVANTAGE - The use of flex tape for the substrate is cheaper to manufacture than laminates and ceramics and the wire bonding for the interconnect of the chip and the substrate is lower in cost has higher flexibility than other interconnects such as TAB bonding. The recess or cavity for attachment of the chip to the **heat spreader** allows for greater protection of the chip and easier assembly of a thin and light package.
Dwg.3/4

L20 ANSWER 7 OF 21 WPIX (C) 2002 THOMSON DERWENT
AN 1998-560253 [48] WPIX
DNN N1998-436911 DNC C1998-167831
TI **Ball grid** array (**BGA**) package for integrated circuits used in e.g. mobile telephones - has a **metal heat** sink **covered** in an insulating sheet including conductive traces, with a central hole into which is mounted the device.
DC A85 L03 U11
IN CHOI, K H; JEONG, T S; LEE, T K; PARK, J S; RYU, K T; YOUN, H S; CHOI, K; JEONG, T; LEE, T; PARK, J; RYU, K; YOUN, H; CHOI, G H; CHUNG, T S; LEE, T G; RYOO, G T; YOON, H S
PA (HYUN-N) HYUNDAI ELECTRONICS IND CO LTD
CYC 7
PI GB 2325340 A 19981118 (199848)* 72p
DE 19821715 A1 19990128 (199910)
CN 1199927 A 19981125 (199915)
JP 11045956 A 19990216 (199917) 16p
KR 98083733 A 19981205 (200007)
KR 98083734 A 19981205 (200007)
US 6060778 A 20000509 (200030)
KR 220249 B1 19990915 (200107)
TW 449844 A 20010811 (200237)
ADT GB 2325340 A GB 1998-6078 19980320; DE 19821715 A1 DE 1998-19821715 19980514; CN 1199927 A CN 1998-107932 19980506; JP 11045956 A JP 1998-100428 19980327; KR 98083733 A KR 1997-19144 19970517; KR 98083734 A KR 1997-19145 19970517; US 6060778 A US 1998-60981 19980415; KR 220249 B1 KR 1997-19144 19970517; TW 449844 A TW 1998-103626 19980312
PRAI KR 1997-19145 19970517; KR 1997-19144 19970517
AB GB 2325340 A UPAB: 19981203
An integrated circuit package comprises an interconnection substrate (50) with a conductive trace layer on each side. A first side (50b) is bonded to a thermally conductive layer (35). The substrate and thermally

conductive layer are essentially square, with a hole (36) in the centre. An integrated circuit device (40) is located in the central hole and connected to bond pads on the conductive traces on the second side of the insulating substrate before being encapsulated (42) and fixed in the hole. **Solder balls** connect to the conductive traces on the second side of the insulating layer. Preferably the first side of the insulating layer has an epoxy or polyimide layer around its periphery. The thermally conductive layer is made from **aluminium** silver or **copper**.

USE - The **ball grid** array package is used for integrated circuit devices used in portable equipment such as mobile telephones, pocket computers etc.

ADVANTAGE - The device package is low-profile, light, cheap to make and has excellent heat dissipation properties.

Dwg.3/15

L20 ANSWER 8 OF 21 JAPIO COPYRIGHT 2002 JPO
AN 2001-313463 JAPIO
TI SUBSTRATE FOR EVALUATING WETTABILITY, AND METHOD FOR EVALUATING WETTABILITY OF BRAZING MATERIAL ELECTRODE
IN FUKUDA YOSHIKI
PA SONY CORP
PI JP 2001313463 A 20011109 Heisei
AI JP 2000-130557 (JP2000130557 Heisei) 20000428
PRAI JP 2000-130557 20000428
SO PATENT ABSTRACTS OF JAPAN (CD-ROM), Unexamined Applications, Vol. 2001
AB PROBLEM TO BE SOLVED: To provide a substrate and method for evaluating, by which the solder wettability of a connection electrode of an electronic component with a **solder ball** as a connection electrode, e.g. such as **BGA** can be evaluated readily under a safe environment and with high reliability.
SOLUTION: An evaluating substrate 10 is provided with wettability evaluating electrodes 11, each being made of a **metal** film which is formed on an end side on one surface of a base material 13. Each evaluating electrode 11 comprises a circular part 11a in one side and a strip part 11b extending from the circuit part 11a to the end edge side of the base material 13. The circular part 11a is used as a melting/fixing electrode for melting and fixing a **solder ball** of a **BGA** component (component electrode). For evaluating wettability, after a component is mounted on the evaluation substrate 10 (the **solder ball** is abutted on the circular part 11a), the **solder ball** is **melted** and the wet **spread** of the solder onto the evaluating electrode is observed visually, so that, wettability of the **solder ball** can be evaluated.
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L20 ANSWER 9 OF 21 JAPIO COPYRIGHT 2002 JPO
AN 1999-186436 JAPIO
TI PLASTIC CIRCUIT BOARD
IN FUKUNAGA NORIKAZU
PA SUMITOMO METAL SMI ELECTRON DEVICES INC
PI JP 11186436 A 19990709 Heisei
AI JP 1997-350729 (JP09350729 Heisei) 19971219
PRAI JP 1997-350729 19971219
SO PATENT ABSTRACTS OF JAPAN (CD-ROM), Unexamined Applications, Vol. 1999
AB PROBLEM TO BE SOLVED: To improve **heat radiation** of a

plastic circuit board.
SOLUTION: An IC chip 12 is loaded on a plastic circuit board 11, and molded by sealing resin 14, and plural **solder balls** 15 are joined to the lower face of the plastic circuit board 11 so that a **PBGA** package 10 can be constituted. A conductive pattern is formed of **copper** foil or the like on the both faces of the plastic circuit board 11. The area ratio of a conductive pattern 16 to the board area is 60% or more, and preferentially, 80% or more. The conductive pattern is formed so that all boundary parts between the adjacent conductive patterns can be thin wires whose thin width is 80 μm (that is, line width which is absolutely necessary for insulation between the conductive patterns). Thus, heat resistance of the plastic circuit board 11 as a whole can be reduced, and the **heat radiation** of an IC chip 12 can be efficiently attained in a path from the plastic circuit board 11 to a printed circuit board 19.
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L20 ANSWER 10 OF 21 JAPIO COPYRIGHT 2002 JPO
AN 1999-163186 JAPIO
TI SEMICONDUCTOR DEVICE
IN TAKANO EIJI; HOSOMI HIDEKAZU; TAKUBO TOMOAKI
PA TOSHIBA CORP
PI JP 11163186 A 19990618 Heisei
AI JP 1997-330210 (JP09330210 Heisei) 19971201
PRAI JP 1997-330210 19971201
SO PATENT ABSTRACTS OF JAPAN (CD-ROM), Unexamined Applications, Vol. 1999
AB PROBLEM TO BE SOLVED: To enable a **BGA** package provided with a cover plate to be warped less, even when a resin board is used.
SOLUTION: A **BGA** package 11 is constituted of a resin **BGA** board 12 and a cover plate 16. A large number of **solder ball** terminals 13 are provided to the underside of the **BGA** board 12, and a chip connecting electrode is formed on the upside of the **BGA** board 12. A semiconductor chip 14 is connected to the electrode in a flip-chip mounting manner. The cover plate 16 is bonded to the **BGA** board 12 with an adhesive agent 17 for covering the semiconductor chip 14, and formed through in such a way that a **copper** plate is bent into the cover plate 16 of an integral structure composed of a top plate 16a and sides 16c connected to the top plate 16a with joints 16b. The **cover** plate 16 is **heated** when it is bonded to the board 12, and a cutout is provided to each of the four corners of the cover plate 16, so that stresses imposed on the **BGA** board 12 can be relaxed, and the board 12 is reduced less.
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L20 ANSWER 11 OF 21 JAPIO COPYRIGHT 2002 JPO
AN 1999-111883 JAPIO
TI SEMICONDUCTOR DEVICE
IN RIKITAKE TOMOTSUGU
PA MITSUI HIGH TEC INC
PI JP 11111883 A 19990423 Heisei
AI JP 1997-287753 (JP09287753 Heisei) 19971003
PRAI JP 1997-287753 19971003
SO PATENT ABSTRACTS OF JAPAN (CD-ROM), Unexamined Applications, Vol. 1999
AB PROBLEM TO BE SOLVED: To provide a semiconductor device for improving **heat radiation** ability without increasing the thickness of a **BGA** type semiconductor device.
SOLUTION: In a semiconductor device for which a semiconductor chip 4 is

loaded on the main surface of a substrate 1 provided with a wiring pattern 2, a terminal 4a of the semiconductor chip and the wiring pattern 2 are electrically connected and resin-sealed and external connection terminals 9 and 12 provided on the back surface side of the substrate 1 and the wiring pattern 2 are connected through a through-hole 10, the external connection terminal 9 provided under the back surface of the semiconductor chip 4 loaded on the substrate 1 is a better heat conductor than the external connection terminal 12 provided in the other area. Also, the external connection terminal 9 provided under the back surface of the semiconductor chip 4 is turned to a **copper** or **copper** alloy ball, and the external connection terminal 12 of the other area is turned to a **solder ball**.
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L20 ANSWER 12 OF 21 JAPIO COPYRIGHT 2002 JPO
AN 1999-097567 JAPIO
TI CAVITY-DOWN TYPE **BGA** PACKAGE
IN NAKADA YOSHIKAZU; TAKAMICHI HIROSHI
PA SUMITOMO METAL SMI ELECTRON DEVICES INC
PI JP 11097567 A 19990409 Heisei
AI JP 1997-256949 (JP09256949 Heisei) 19970922
PRAI JP 1997-256949 19970922
SO PATENT ABSTRACTS OF JAPAN (CD-ROM), Unexamined Applications, Vol. 1999
AB PROBLEM TO BE SOLVED: To improve the adhesive force and the **heat radiation** of a plurality of **metal** plates constituting the **heat-radiation** slug of a cavity-down type **BGA** package.
SOLUTION: A **heat-radiation** 21 is constituted by a planar **metal** plate 22 and a **metal** plate 23 having a punched opening for a cavity 24 in the center, these two **metal** plates 22, 23 being bonded with brazing material 25 such as AgCu. A plastic circuit board 26 is bonded to the bottom surface of the **heat- radiating** slug 21 via an adhesive resin sheet 27 and many **solder balls** 28 as connecting electrodes are arranged on the bottom surface of the plastic circuit board 26. A semiconductor chip 30 is die-bonded to the cavity 24 of the **heat - radiation** slug 21, the semiconductor chip 30 is connected to the plastic circuit board 26 with a bonding wire 31, and then the cavity 24 is filled with sealing resin 32. In this case, the **metal** plates 22, 23 are bonded to each other with brazing material 25 to improve the adhesive force and heat dissipation.
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L20 ANSWER 13 OF 21 JAPIO COPYRIGHT 2002 JPO
AN 1999-067968 JAPIO
TI **BALL GRID** ARRAY PACKAGE, MANUFACTURE THEREOF AND PRINTED CIRCUIT BOARD THEREFOR
IN AN INTETSU; KA YUKI; RI EIBIN
PA SAMSUNG ELECTRON CO LTD
PI JP 11067968 A 19990309 Heisei
AI JP 1998-49245 (JP10049245 Heisei) 19980302
PRAI KR 1997-38466 19970812
SO PATENT ABSTRACTS OF JAPAN (CD-ROM), Unexamined Applications, Vol. 1999
AB PROBLEM TO BE SOLVED: To avoid moisture absorption through **heat radiating** vias and improve **heat radiation**, by filling these vias with a **metal** having a high thermal conductivity and low moisture absorption.

SOLUTION: A package 200 comprises a printed circuit board 110 having a chip mounting region 160 and a circuit pattern 15, a semiconductor chip mounted on the mounting region 160, bonding wires 140 for electrically connecting the semiconductor chip to a circuit pattern 115, a package body 150 formed with the sealed semiconductor chip and the bonding wires 140, and **solder balls** 130. **Heat radiating** vias 162a are formed in a lower part of the chip-mounting region 160 to **radiate** out the **heat** generated during operating of the chip and filled with a low-m.p. **metal** 172 to avoid penetrating the water content in the package body, and to improve the **heat radiation**.
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L20 ANSWER 14 OF 21 JAPIO COPYRIGHT 2002 JPO
AN 1999-054656 JAPIO
TI MANUFACTURE OF SOLDER BUMP ELECTRODE AND SOLDER BUMP ELECTRODE
IN ITO KATSUMI
PA NEC CORP
PI JP 11054656 A 19990226 Heisei
AI JP 1997-220972 (JP09220972 Heisei) 19970731
PRAI JP 1997-220972 19970731
SO PATENT ABSTRACTS OF JAPAN (CD-ROM), Unexamined Applications, Vol. 1999
AB PROBLEM TO BE SOLVED: To provide a method of manufacturing solder bump electrodes that can maintain a predetermined interval between a substrate and a package and permit stable mounting, even if there are variations in mounting temperature by providing a structure, in which a high melting-point **solder ball** or conductive **metal** ball is **covered** with a low **melting**-point **solder ball** and by making the size of the high melting-point **solder ball** or conductive **metal** ball equal to a desired predetermined interval, in a **BGA** package.
SOLUTION: An opening is formed only at a terminal portion 2 in a solder resist 1 which is applied over the entire surface of a package substrate 3. A small quantity of liquid high melting point solder 4 is dropped. Such a small quantity of solder 4 becomes spherical by the surface tension and solidifies. An appropriate quantity of liquid low melting point solder 6 is dropped, so that a low melting point **solder ball** 7 is formed so as to **cover** the high **melting** point **solder ball** 5 formed as described.
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L20 ANSWER 15 OF 21 JAPIO COPYRIGHT 2002 JPO
AN 1999-026658 JAPIO
TI PACKAGE STRUCTURE OF **BGA** SEMICONDUCTOR DEVICE
IN KAKU YOSHITAKA
PA ROHM CO LTD
PI JP 11026658 A 19990129 Heisei
AI JP 1997-184203 (JP09184203 Heisei) 19970709
PRAI JP 1997-184203 19970709
SO PATENT ABSTRACTS OF JAPAN (CD-ROM), Unexamined Applications, Vol. 1999
AB PROBLEM TO BE SOLVED: To improve the radiation efficiency of a package to avoid damaging a semiconductor due to the heat staying therein by roughening the surface of the package for the **heat radiation**.
SOLUTION: The **BGA** semiconductor device has a chip 2 fixed to a substrate 1 and **solder balls** 5 on the substrate

surface are made conductive to the chip through inner leads 4 by the wire bonding 3. On the substrate, a resin-molded package P is formed and has a rough surface M to increase the radiation area. Such rough surface M increases the package surface area enough to well **radiate** the **heat** staying in the package P. A **Cu** heat sink is adhered to the inner bottom of a recess to more improve the **radiation** efficiency. The **heat** sink may be contacted to the chip 2 on the substrate 1 to much **radiate** the **heat** staying in the chip 2.
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L20 ANSWER 16 OF 21 JAPIO COPYRIGHT 2002 JPO
AN 1999-003957 JAPIO
TI THIN-FILM POWER TAPE **BALL GRID** ARRAY PACKAGE
IN CHIA CHOK J; VARIOT PATRICK; ALAGARATNAM MANIAM
PA LSI LOGIC CORP
PI JP 11003957 A 19990106 Heisei
AI JP 1998-109632 (JP10109632 Heisei) 19980420
PRAI US 1997-840614 19970421
SO PATENT ABSTRACTS OF JAPAN (CD-ROM), Unexamined Applications, Vol. 1999
AB PROBLEM TO BE SOLVED: To provide a **ball grid** array package which is economical and high in its density.
SOLUTION: An integrated circuit package 2 includes a **heat spreader** 4 formed to have a central recess face 16 between its flat faces 12 and 14, and also includes flexible tapes extended from the flat faces 12 and 14 to the central recess face 16. A semiconductor chip 24 is mounted on the central recess face 16 between the flexible tapes and then, by wire bonding, the bonding pads of the chip 24 are interconnected to a **metal** interconnect pattern of the tapes. Then plastic molding or epoxy is applied to seal the chip and wire bonding on the central recess face of the **heat spreader** 4. Thereby the package 2 can be easily mounted on a motherboard by means of **solder balls**.
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L20 ANSWER 17 OF 21 JAPIO COPYRIGHT 2002 JPO
AN 1998-247702 JAPIO
TI **BALL GRID** ARRAY PACKAGE AND PRINTED BOARD
IN FUKUNAGA NORIKAZU
PA SUMITOMO KINZOKU ELECTRO DEVICE:KK
PI JP 10247702 A 19980914 Heisei
AI JP 1997-69157 (JP09069157 Heisei) 19970305
PRAI JP 1997-69157 19970305
SO PATENT ABSTRACTS OF JAPAN (CD-ROM), Unexamined Applications, Vol. 1998
AB PROBLEM TO BE SOLVED: To improve the **heat radiating** property, by a method wherein a **heat radiating** board in excellent **thermal** conductivity is junctioned with the bottom face side of the semiconductor element mounting part of a resin substrate having the semiconductor element mounting part on the top face side, with the junctioning **pad** of a **solder ball** on the bottom face side.
SOLUTION: A **ball grid** array package 10 is provided with a resin substrate 13 having the mounting part of a semiconductor element 11 on the top face side thereof while having a **solder ball** junctioning **pad** on the bottom face side thereof. On the other hand, a **heat radiating** board 21 in excellent thermal conductivity is junctioned with the bottom face side of the

semiconductor element mounting part of the resin substrate 13. Resultantly, the heat dissipated from the bottom face of the semiconductor element 1 is radiated to a printed substrate 41 in almost the shortest distant path. Besides, the **heat radiating** board 21 formed of a material in excellent thermal conductivity such as **copper**, etc., also takes a planar shape at the lower thermal resistance, thereby enabling the semiconductor element 11 to efficiently **radiate** the **heat** to the printed wiring board 41.
COPYRIGHT: (C)1998,JPO

L20 ANSWER 18 OF 21 JAPIO COPYRIGHT 2002 JPO
AN 1998-200012 JAPIO
TI PACKAGE OF **BALL GRID** ARRAY SEMICONDUCTOR AND ITS MANUFACTURING METHOD
IN KYO EIKYOKU; CHIN ITSUKKEN; ROBERT DAVYWOOKS
PA ANAM IND CO INC
PI JP 10200012 A 19980731 Heisei
AI JP 1997-233372 (JP09233372 Heisei) 19970814
PRAI KR 1996-77898 19961230
KR 1996-77899 19961230
KR 1997-4430 19970214
SO PATENT ABSTRACTS OF JAPAN (CD-ROM), Unexamined Applications, Vol. 1998
AB PROBLEM TO BE SOLVED: To provide a lighter and thinner package while improving electrical performance and **heat-radiation** characteristics, and to remove such phenomenon as package bending, by bonding a flexible circuit board to the bottom surface of a semiconductor chip, and connecting a pad to a circuit pattern with a wire for sealing, etc.
SOLUTION: On the bottom surface of a semiconductor chip 51 wherein multiple input/output pads 52 are formed on its surface, a flexible circuit board 20 wherein a circuit pattern 21 is formed on a flexible resin film 22 is bonded through a bonding layer 60. Further, the input/output pad 52 of the semiconductor chip 51 is connected to the circuit pattern 21 of the flexible circuit board 20 with a conductive wire 53, and the semiconductor chip 51 and the conductive wire 53 are, for protection from external environment, sealed up with a sealing part 40. At the bottom surface of flexible circuit board 20, multiple **solder balls** 30 are fused as input/output terminal. In addition, a **metal** outside supporting plate 16, for example, may be bonded to the upper-surface outside periphery of the flexible circuit board 20.
COPYRIGHT: (C)1998,JPO

L20 ANSWER 19 OF 21 JAPIO COPYRIGHT 2002 JPO
AN 1998-125833 JAPIO
TI **BGA** TYPE PACKAGE MOUNTING SUBSTRATE AND **BGA** TYPE PACKAGE MOUNTING METHOD
IN HASEGAWA TAKAHIKO
PA DENSO CORP
PI JP 10125833 A 19980515 Heisei
AI JP 1996-280925 (JP08280925 Heisei) 19961023
PRAI JP 1996-280925 19961023
SO PATENT ABSTRACTS OF JAPAN (CD-ROM), Unexamined Applications, Vol. 1998
AB PROBLEM TO BE SOLVED: To test the solder bond condition using an X-ray, and improve the **heat radiation** power using a **metal**-made heat dissipation member.
SOLUTION: A circuit board 30 has heat dissipation through-holes 34 for transmitting the heat transmitted through **solder balls**

20 from a **BGA**(**ball grid** array) package 1 to the substrate back side. The package 1 is disposed on the surface of the circuit board 30 and soldered by the solder reflow method. The solder bond condition of the board 30 to the package 1 is inspected by the X-ray. After the inspection, a heat dissipation member 40 for dissipating the heat transmitted from the through-holes 34 of the board 30 is mounted on the back surface of the board 30.
COPYRIGHT: (C)1998,JPO

L20 ANSWER 20 OF 21 JAPIO COPYRIGHT 2002 JPO
AN 1998-084057 JAPIO
TI **BGA** SEMICONDUCTOR PACKAGE WITH **METAL** CARRIER FRAME AND MANUFACTURE THEREOF
IN CHIN ICHIKEN; KYO EIKYOKU
PA ANAM IND CO INC
PI JP 10084057 A 19980331 Heisei
AI JP 1997-19725 (JP09019725 Heisei) 19970117
PRAI KR 1996-5345 19960229
SO PATENT ABSTRACTS OF JAPAN (CD-ROM), Unexamined Applications, Vol. 1998
AB PROBLEM TO BE SOLVED: To enable a **BGA** semiconductor package to dissipate heat easily so as to improve it in reliability by a method wherein a **metal** carrier frame is partially exposed to the outside and attached to the package to serve as a **heat spreader**.
SOLUTION: A **BGA** semiconductor package is composed of a semiconductor chip 20 and a PCB board 10 mounted with the chip 10, wherein chip pads on the semiconductor chip 20 and a circuit pattern 11 formed on the upside of the PCB board 10 are bonded together with wires 30 respectively, and the semiconductor chip 20 is sealed up with a sealing compound 40 so as to be protected against oxidation and corrosion from the outside. A large number of **solder balls** 50 are attached to the base of the PCB board 10, and a PCB board support 64 as a part of a **metal** carrier frame is attached to the outer upside of the PCB board 10 outside a region sealed up with the sealing compound 40 to function as a **heat spreader**. Therefore, **heat** released from the circuit of a semiconductor chip in the operation can easily be dissipated out into the air.
COPYRIGHT: (C)1998,JPO

L20 ANSWER 21 OF 21 JAPIO COPYRIGHT 2002 JPO
AN 1997-321085 JAPIO
TI SEMICONDUCTOR DEVICE AND ITS ASSEMBLING METHOD
IN OYA NOBUAKI; OKUTOMO TAKAYUKI; TAGUCHI HIDEO; IKEMIZU MORIHIKO
PA TOSHIBA CORP
PI JP 09321085 A 19971212 Heisei
AI JP 1996-136287 (JP08136287 Heisei) 19960530
PRAI JP 1996-136287 19960530
SO PATENT ABSTRACTS OF JAPAN (CD-ROM), Unexamined Applications, Vol. 1997
AB PROBLEM TO BE SOLVED: To suppress the occurrence of cracks caused by heat, at the **solder ball** of a **BGA** package type semiconductor device which has **heat radiation** member, by partially bonding a **heat radiation** member to a flattening member.
SOLUTION: This semiconductor device is provided with a chip carrier 1 which has a group of ball-shaped electrodes 9, a semiconductor integrated circuit chip 5 which is electrically connected to the chip carrier 1 and in which the group of ball-shaped electrodes 9 serve as external

terminals, and a flattening member 2 for keeping the flatness of the chip carrier 1. Furthermore, this is provided with a heat dissipating member 7 for letting go the heat generated from the semiconductor integrated circuit 5, being thermally coupled with the semiconductor integrated circuit chip 5. Then, the heat dissipating member 7 is bonded partially to the flattening member 2. For example, a stainless fastener is bonded by an adhesive 3 onto the TAB tape 1, and thereon a **copper** cover plate 7 is bonded partially only at a projection 12 for bonding by an adhesive 8.

L23 ANSWER 1 OF 1 WPIX (C) 2002 THOMSON DERWENT
AN 1997-134660 [13] WPIX
CR 2001-111822 [08]
DNN N1997-111019
TI Flip-chip for e.g. reflow solder attachment to chip carrier esp. in **BGA** module - includes conductive high melting temp. metal bumps on pads, which are in turn covered with bumps of low joining temp., joining material e.g. solder paste suitable for bonding to carrier.
DC U11
IN FALLON, K M; LE COZ, C R; PIERSON, M V
PA (IBMC) INT BUSINESS MACHINES CORP
CYC 7
PI EP 757386 A2 19970205 (199713)* EN 89p
R: DE FR GB IE
KR 97012964 A 19970329 (199815)
US 5872051 A 19990216 (199914)
KR 257420 B1 20000515 (200128)
CN 1152190 A 19970618 (200132)
ADT EP 757386 A2 EP 1996-305563 19960730; KR 97012964 A KR 1996-28556 19960715; US 5872051 A US 1995-510401 19950802; KR 257420 B1 KR 1996-28556 19960715; CN 1152190 A CN 1996-109910 19960712
PRAI US 1995-510401 19950802
AB EP 757386 A UPAB: 20010611
The integrated circuit chip includes electronic devices formed in a semiconductor substrate surface, with at least two wiring layers connected to the devices. The wiring layers, separated by dielectric layers, include flat conductive metal pads of high melting temp. on the surface. A passivation layer covers the surface, with **windows** at the pads. Bumps of a different, conductive, **high melting temp**. metal **cover** the pads.

There are bumps of a low joining temp., joining material on the high melting temp. bumps, having a joining temp. sufficiently lower than the melting temp. of the metal for joining to connectors of a carrier without melting the high melting temp. metal. The pad bumps may be uncured solder paste with a joining temp. sufficiently lower than the pad melting temp. for reflow solder attachment without melting the pads.

L24 ANSWER 1 OF 34 WPIX (C) 2002 THOMSON DERWENT
AN 2002-390647 [42] WPIX
TI Semiconductor package.
DC U11
IN KIM, S M
PA (AMKO-N) AMKOR TECHNOLOGY KOREA INC
CYC 1
PI KR 2001111768 A 20011220 (200242)* 1p
ADT KR 2001111768 A KR 2000-32433 20000613
PRAI KR 2000-32433 20000613
AB KR2001111768 A UPAB: 20020704
NOVELTY - A semiconductor package is provided to maximize a heat emission efficiency by applying a **heat spreader** in a **BGA** semiconductor package using a PCB member.
DETAILED DESCRIPTION - In a semiconductor package, a resin layer(30) is provided. A conductive pattern(24) is formed and attached on the resin layer. A chip(28) is packaged in an area for loading a chip formed on the resin layer. A wire(38) is connected between a bonding area of the conductive pattern and a **bonding pad** of the chip. A molded resin(34) is provided to protect the chip, the wire and the bonding area of the conductive pattern from the exterior. A part of a solder mask (22) layer outside the area for loading a chip is incised to expose the conductive pattern. A **heat spreader**(10) having a cap form is attached to the exposed conductive pattern plane with a bonding means(32) having a good **thermal conductivity**, while the resin is molded thereon as to expose the upper plane of the **heat spreader** to the exterior.
Dwg.1/10

L24 ANSWER 2 OF 34 WPIX (C) 2002 THOMSON DERWENT
AN 2002-273086 [32] WPIX
DNN N2002-212855
TI Failure analysis method of semiconductor device, involves **bonding pad** on semiconductor chip and output pad for analysis, by wire.
DC S01 U11
IN OZAWA, T
PA (NIDE) NEC CORP
CYC 2
PI JP 2001289905 A 20011019 (200232)* 5p
US 2002013009 A1 20020131 (200232)
ADT JP 2001289905 A JP 2000-104457 20000406; US 2002013009 A1 US 2001-822368 20010402
PRAI JP 2000-104457 20000406
AB JP2001289905 A UPAB: 20020521
NOVELTY - The **heat spreader** and micro solder balls are provided to top and bottom surfaces of silicon substrate. While performing failure analysis, the solder ball for **BGA** provided in undersurface of ceramic substrate, and ceramic substrate are removed, and then micro solder ball is removed to expose pad of silicon substrate, connected with output **pad** by **bonding** wires.
USE - For failure analysis of semiconductor device of flip-chip type.
ADVANTAGE - Since failure analysis is performed by **bonding** required **pads**, effective electric and physical failure analysis of semiconductor device is enabled.
DESCRIPTION OF DRAWING(S) - The figure shows a flowchart of failure

analysis process. (Drawing includes non-English language text).
Dwg.1/9

L24 ANSWER 3 OF 34 WPIX (C) 2002 THOMSON DERWENT
AN 2002-194437 [25] WPIX
CR 1999-142093 [12]; 2001-535495 [56]
DNN N2002-147613
TI Semiconductor assembly has recess with **heat** dissipating glob top **covering** one surface of semiconductor chip.
DC U11
IN AKRAM, S; WARK, J M
PA (MICR-N) MICRON TECHNOLOGY INC
CYC 1
PI US 6252308 B1 20010626 (200225)* 13p
ADT US 6252308 B1 Cont of US 1996-653030 19960524, US 1998-189102 19981109
FDT US 6252308 B1 Cont of US 5866953
PRAI US 1996-653030 19960524; US 1998-189102 19981109
AB US 6252308 B UPAB: 20020418
NOVELTY - The semiconductor assembly has a semiconductor chip (402) with surface (406) attached to and in electrical communication with substrate (416). A barrier glob top (424) is adhered to periphery and edges of another surface of the chip to form a wall so that it extends and contacts substrate.

DETAILED DESCRIPTION - A recess (426) with heat dissipating glob top (428) is defined by the wall so that it covers periphery of another surface of chip.

An INDEPENDENT CLAIM is also included for method for producing semiconductor assembly.

USE - For attaching semiconductor devices such as **ball grid** array (**BGA**), pin grid array (PGA) to printed circuit board including flip-chip attachment, wire bonding and tape automated wire bonding (TAB) using chip-on-board (COB) technique.

ADVANTAGE - Provides adherence and sealing benefits of low **thermal conductivity** glob top and the benefits of heat dissipation provided by a high **thermal conductivity** glob top.

DESCRIPTION OF DRAWING(S) - The figure shows the side cross-sectional view of encapsulated semiconductor assembly.

Semiconductor chip 402
Surface 406
Substrate 416
Barrier glob top 424
Recess 426
Heat dissipating glob top 428
Dwg.4/9

L24 ANSWER 4 OF 34 WPIX (C) 2002 THOMSON DERWENT
AN 2001-591444 [67] WPIX
DNN N2001-440684
TI **Heat radiation** fin for **ball grid** array semiconductor device, has several **heat radiation** plates made of **heat** resistant resin having carbon fibers, mounted on substrate.
DC U11
IN MURAYAMA, K; HIGASHI, M; KOIKE, H; SAKAGUCHI, H
PA (SHIA) SHINKO ELECTRIC IND CO LTD; (SHIA) SHINKO DENKI KOGYO KK; (HIGA-I) HIGASHI M; (KOIK-I) KOIKE H; (MURA-I) MURAYAMA K; (SAKA-I) SAKAGUCHI H

CYC 28
PI EP 1122779 A2 20010808 (200167)* EN 13p
R: AL AT BE CH CY DE DK ES FI FR GB GR IE IT LI LT LU LV MC MK NL PT RO SE SI TR
JP 2001217359 A 20010810 (200167) 8p
EP 1122779 A8 20020403 (200223) EN
R: AL AT BE CH CY DE DK ES FI FR GB GR IE IT LI LT LU LV MC MK NL PT RO SE SI TR
US 2002062946 A1 20020530 (200240)
ADT EP 1122779 A2 EP 2001-300605 20010124; JP 2001217359 A JP 2000-21914 20000131; EP 1122779 A8 EP 2001-300605 20010124; US 2002062946 A1 Div ex US 2001-767432 20010123, US 2002-43943 20020110
PRAI JP 2000-21914 20000131
AB EP 1122779 A UPAB: 20011119
NOVELTY - Several **heat radiation** plates (12) are mounted vertically on the substrate (11) of high **thermal conductivity**, at predetermined intervals. Each **heat radiation** plate is made of heat resistant resin containing carbon fibers.
DETAILED DESCRIPTION - INDEPENDENT CLAIMS are also included for the following:
(a) **Heat radiation** fin manufacturing method;
(b) Semiconductor device
USE - For use in e.g. **ball grid** array (**BGA**), pin grid array (PGA) semiconductor devices.
ADVANTAGE - **Heat radiation** effect is maintained with high efficiency using the **heat radiation** plates made of high resistive resin containing carbon fibers.
DESCRIPTION OF DRAWING(S) - The figure shows the structure of **heat radiation** fin.
Substrate 11
**Heat radiation** plates 12
Dwg.2/7

L24 ANSWER 5 OF 34 WPIX (C) 2002 THOMSON DERWENT
AN 2001-585957 [66] WPIX
DNN N2001-437009
TI Tape automated bonding tape for **ball grid** array semiconductor device, has dummy solder resist areas and circuit wiring structure between signal, power supply and lead wirings.
DC U11
PA (HITD) HITACHI CABLE LTD
CYC 1
PI JP 2001144146 A 20010525 (200166)* 9p
ADT JP 2001144146 A JP 1999-319731 19991110
PRAI JP 1999-319731 19991110
AB JP2001144146 A UPAB: 20011113
NOVELTY - Dummy solder resist areas (31,32) and circuit wiring structure (24) are provided between the signal wiring (4), power supply wiring (5) and lead wiring (53) in the area ranging from the **bonding pad** section (23) of TAB tape surface, to the device hole (26).
DETAILED DESCRIPTION - An INDEPENDENT CLAIM is also included for the semiconductor device.
USE - Tape automated bonding (TAB) tape for **ball grid** array (**BGA**) semiconductor device (claimed).
ADVANTAGE - Generation of gap between the TAB tape and the adhesive agent is prevented, hence reliability and **heat radiation**

property are improved.
DESCRIPTION OF DRAWING(S) - The figure shows the detailed diagram of TAB tape.
Signal wiring 4
Power supply wiring 5
**Bonding pad** section 23
Circuit wiring structure 24
Device hole 26
Dummy solder resist areas 31,32
Lead wiring 53
Dwg.1/6

L24 ANSWER 6 OF 34 WPIX (C) 2002 THOMSON DERWENT
AN 2001-474878 [51] WPIX
CR 2001-464390 [50]
DNN N2001-351462 DNC C2001-142314
TI Application of thermoplastic polymer to semiconductor component, e.g. printed circuit board, to form bonding layers involves applying dispersion comprising thermoplastic particles and liquid medium.
DC A85 L03 U11
IN COBBLEY, C A; JIANG, T; VANNORTWICK, J
PA (MICR-N) MICRO TECHNOLOGY INC
CYC 1
PI US 6238223 B1 20010529 (200151)* 16p
ADT US 6238223 B1 US 1997-915211 19970820
PRAI US 1997-915211 19970820
AB US 6238223 B UPAB: 20010910
NOVELTY - A thermoplastic polymer is applied to a semiconductor component by providing a dispersion comprising thermoplastic particles and liquid medium. The dispersion is applied on the surface of semiconductor component and then dried.
DETAILED DESCRIPTION - An INDEPENDENT CLAIM is also included for the formation of an array of conductive thermoplastic deposits on molded body surface of integrated circuit package.
USE - For applying thermoplastic polymer to semiconductor component e.g. wafers, dies, leadframe, lead fingers, wire bonds and printed circuit board or flip chip mounted on printed circuit board to form **bonding** layers (15), **pads** or bumps. It is useful in surface mount attachment of devices (10) to e.g. printed circuit boards (14), chip-on board (COB), lead on chip (LOC), direct chip attach (DCA) and **ball grid** arrays (**BGA**).
ADVANTAGE - Conveniently deposits material by screen or stencil printing in semiconductor packaging applications so preventing damage on screen. The working life of dispersion is increased because the thermoplastic polymer does not cure as solvent evaporates. The process provides reliable bonding materials which provide good performance properties and exhibit economical processing features. The process allows for higher throughput and better economy in producing semiconductor packages.
DESCRIPTION OF DRAWING(S) - The drawing shows a diagram of a device mounted on printed circuit board.
Devices 10
Printed circuit boards 14
Bonding layer 15
Dwg.1/9

L24 ANSWER 7 OF 34 WPIX (C) 2002 THOMSON DERWENT

AN 2001-127125 [14] WPIX
DNC C2001-037181
TI **Thermally conductive** adhesive for attaching semiconductor package to heat sink, comprises anti-magnetic filler of specific heat conductivity mixed with adhesive polymer.
DC A14 A28 A85 G03 L03
PA (FUJI-N) FUJI POLYMERTECH KK
CYC 1
PI JP 2000273426 A 20001003 (200114)* 8p
ADT JP 2000273426 A JP 1999-85107 19990329
PRAI JP 1999-85107 19990329
AB JP2000273426 A UPAB: 20010312
NOVELTY - The adhesive (3) comprises an anti-magnetic filler (whose magnetism is comparable with a ferromagnetic material) of heat conductivity 20 W/m.K or more, mixed with an adhesive polymer.
DETAILED DESCRIPTION - INDEPENDENT CLAIMS are also included for:
(i) attachment method of the adhesive with the adherent. The adhesive is applied between the adherents and the filler is oriented in a fixed direction by an external magnetic field; and
(ii) semiconductor device.
USE - For attaching semiconductor package (2) with **heat radiators** (4) such as **heat** sink and for attaching semiconductor chip with die pad, for semiconductor devices used in electrical equipment, power supply, light source, etc.
ADVANTAGE - Heat conductivity and heat release property of the adhesive are improved.
DESCRIPTION OF DRAWING(S) - The figure shows the attachment method of **ball grid** array type semiconductor package with **heat radiator** using the adhesive.
Semiconductor package 2
Thermal conducting adhesive 3
**Heat radiator** 4
Dwg.1/8

L24 ANSWER 8 OF 34 WPIX (C) 2002 THOMSON DERWENT
AN 2000-646468 [62] WPIX
DNN N2000-479064 DNC C2000-195440
TI **Heat spreader** removal from integrated circuit package to access circuit chip encapsulated within a device package using abrasion combined with nitric acid solution.
DC L03 P78 S01 U11
IN SCOTT, S E; WEAVER, K
PA (LSIL-N) LSI LOGIC CORP
CYC 1
PI US 6117352 A 20000912 (200062)* 8p
ADT US 6117352 A US 1997-975025 19971120
PRAI US 1997-975025 19971120
AB US 6117352 A UPAB: 20001130
NOVELTY - **Heat spreader** (30) is removed from an integrated circuit chip encapsulated within a device package (10), exposing the chip and inside of the package.
DETAILED DESCRIPTION - Exposing IC housed in a package (10) comprises:
(i) providing a substrate of dielectrically spaced contacts electrically coupled to the IC and terminating upon a surface of the substrate (14), providing a **thermally conductive heat spreader** (30);

(ii) arranging masking material adjacent to an exposed horizontal surface of the **heat spreader**, so a cavity extending through the masking material is aligned to the IC; and

(iii) forwarding a **heat spreader** etchant through a conduit to the cavity and upon an exposed portion of the horizontal surface of the spreader to remove part of the spreader which extends vertically through the **heat spreader**.

USE - For IC manufacture.

DESCRIPTION OF DRAWING(S) - The drawing shows a cross-sectional view of a **BGA** device package.

package 10

substrate 14

**heat spreader** 30

Dwg.4/6

L24 ANSWER 9 OF 34 WPIX (C) 2002 THOMSON DERWENT

AN 2000-364290 [31] WPIX

DNN N2000-272620 DNC C2000-109842

TI Integrated circuit package e.g. **ball grid** array package has flex tape which has conductive metal lead pattern positioned on side of tape facing substrate with apertures, exposes lead pattern for solder ball bonding.

DC A85 L03 U11

IN ALAGARATNAM, M; CHIA, C J; LOW, Q H

PA (LSIL-N) LSI LOGIC CORP

CYC 1

PI US 6057594 A 20000502 (200031)* 5p

ADT US 6057594 A US 1997-842379 19970423

PRAI US 1997-842379 19970423

AB US 6057594 A UPAB: 20000630

NOVELTY - IC package has molded plastic base structure sandwiched between heat conductive substrate (4) and flex tape (16). Flex tape has conductive metal lead pattern (18) positioned on tape side facing substrate with apertures (22) that exposes lead pattern for solder ball bonding. Semiconductor IC (12) is mounted on central point of **heat spreader** (10). Chip and wiring bonding are then encapsulated on substrate.

DETAILED DESCRIPTION - A molded plastic base structure includes heat conductive substrate and flex tape extending from corresponding side of substrate. The heat conductive substrate is laminate structure comprising metal and ceramics. The molded plastic material is present between substrate and flex tape which has conductive metal lead pattern on the tape side which faces the substrate. Apertures exposes conductive lead pattern for solder ball bonding. A semiconductor IC chip with active and non-active side is mounted to central portion of **heat spreader** and active side has bond pads (14) for interconnecting integrated circuit. Wire **bonding** interconnects bond **pads** on clip to metal lead pattern chip. The wire bonding are then encapsulated on substrate by filling cavity in the substrate partially by a resin. The cavity has molded plastic along its side walls. The flex tape also extends along side walls of cavity.

USE - For large scale integrated (LSI) circuits, integrated circuit (IC) packages e.g. **ball grid** array (**BGA**) package, formed by tape automated bonding (TAB).

ADVANTAGE - As chip is directly fixed to **heat spreader heat** dissipation is increased. Wire bonding is lower in cost and has flexibility higher then tape automated bonding (TAB)

hence resulting package is economical to manufacture, thin and light weight.

DESCRIPTION OF DRAWING(S) - The figure shows perspective view of **ball grid** array package.

Heat conductive substrate 4

**Heat spreader** 10

Semiconductor integrated chip 12

Bond pads 14

Flex tape 16

lead pattern 18

Apertures 22

Dwg.3/5

L24 ANSWER 10 OF 34 WPIX (C) 2002 THOMSON DERWENT

AN 2000-292302 [25] WPIX

DNN N2000-219211 DNC C2000-088184

TI **Ball grid** array integrated circuit package has second adhesive with higher **thermal conductivity** and lower bond strength than first adhesive.

DC A85 L03 U11

IN DIBBLE, E P; JOHNSON, E A; PHILLIPS, R A

PA (IBMC) IBM CORP; (IBMC) INT BUSINESS MACHINES CORP

CYC 4

PI US 6040631 A 20000321 (200025)* 5p

CN 1262524 A 20000809 (200055)

KR 2000053485 A 20000825 (200121)

SG 89309 A1 20020618 (200253)

ADT US 6040631 A US 1999-238872 19990127; CN 1262524 A CN 1999-125350 19991217; KR 2000053485 A KR 2000-1612 20000114; SG 89309 A1 SG 1999-6327 19991210

PRAI US 1999-238872 19990127

AB US 6040631 A UPAB: 20000524

NOVELTY - First (18) and second (20) adhesives are attached to respective first and second portions of chip connection surfaces (22) and **heat spreader** connection surfaces (20). The second adhesive has higher **thermal conductivity** and lower bond strength than the first adhesive.

USE - For a **ball grid** array (**BGA**) integrated circuit package.

ADVANTAGE - The bonding system can accommodate higher stresses without significantly increasing the package's thermal resistance, and is simple and inexpensive to produce.

DESCRIPTION OF DRAWING(S) - The drawing shows a cross section of the **ball grid** array integrated circuit package.

**heat spreader** 12

chip 14

first adhesive 16

second adhesive 18

**heat spreader** connection surface 20

chip connection surface 22

Dwg.1/3

L24 ANSWER 11 OF 34 WPIX (C) 2002 THOMSON DERWENT

AN 2000-255583 [22] WPIX

DNN N2000-189954 DNC C2000-077909

TI Forming **thermal conductive** structure on printed circuit board (PCB) includes forming a **heat spreader**

on its surface, forming a glue layer over the **heat spreader** and attaching a surface metallic layer to the spreader and the glue layer.

DC L03 V04
IN JEN, J; TZENG, T; CHENG, D C H; TSENG, T
PA (WORL-N) WORLD WISER ELECTRONICS INC
CYC 2
PI US 6032355 A 20000307 (200022)* 11p
TW 388201 A 20000421 (200061)
ADT US 6032355 A US 1998-130360 19980806; TW 388201 A TW 1998-106140 19980422
PRAI TW 1998-106140 19980422
AB US 6032355 A UPAB: 20000508
NOVELTY - A **thermal conductive** structure is formed on a PCB comprises forming a **heat spreader** (402) having an embossed pattern formed on its surface, after which an adhesive glue layer (404) is attached to the **heat spreader**. A surface metallic layer (406) is attached to the **heat spreader** and the glue layer, in which a portion of its layer is in direct contact with the **heat spreader**.

DETAILED DESCRIPTION - A method of manufacturing a **thermal conductive** structure on a PCB, comprises (a) attaching a **heat spreader** formed on the PCB; (b) forming a first embossed pattern on a portion of the surface of the **heat spreader**; (c) forming a second embossed pattern on the edge portion of the surface of the **heat spreader**; (d) forming an adhesive glue layer to the **heat spreader**; (e) attaching a surface metallic layer to the **heat spreader** and the adhesive glue layer, where a portion of the surface metallic layer is in direct contact or almost direct contact with the first and the second embossed portions of the **heat spreader**; and (g) mounting an external heat sink (514) on top of the surface metallic layer where corresponding to the second embossed pattern of the edge of the **heat spreader**.

USE - The method is used for forming a **thermal conductive** structure on a PCB. The **thermal conductive** structure can also be applied to **ball grid** array packages, chip scale packages and multi-chip modules.

ADVANTAGE - The **thermal conductive** path dissipating heat is reduced considerably and the resulting heat dissipation is very much faster. Since no extra material is required for forming these structures and the method of fabrication is quite simple, the structure can be mass-produced at a very low cost.

DESCRIPTION OF DRAWING(S) - The figure shows a cross-sectional view showing a package structure having an additional external heat sink.

**Heat spreader** 402
Adhesive glue layer 404
Surface metallic layer 406
Heat sink 514
Dwg.5/8

L24 ANSWER 12 OF 34 WPIX (C) 2002 THOMSON DERWENT
AN 1999-600911 [51] WPIX
DNN N1999-442960
TI **Heat spreader** slug used with **heat** sink for dissipating heat in electronic components.
DC V04
IN BARNES, R; KIM, D K J; MARSHALL, B

PA (SUNM) SUN MICROSYSTEMS INC
CYC 1
PI US 5969949 A 19991019 (199951)* 6p
ADT US 5969949 A US 1998-52817 19980331
PRAI US 1998-52817 19980331
AB US 5969949 A UPAB: 19991207
NOVELTY - The slug (16) is interposed between the base (22) of the heat sink (21) and a chip (12) mounted on a substrate (11). The upper surface of slug is formed with longitudinally extending tongue (18) and several tapped holes (19) formed in tongue (18). A longitudinal groove (26) is formed in the base of heat sink which mates with the tongue to align the heat sink with slug.

DETAILED DESCRIPTION - The base (22) is formed with an upward offset (27) above the groove (26). Holes are formed in offset (27) in alignment with holes (19) so that screws (31) are inserted through the holes (28,19) for detachably securing heat sink (21) to slug (16). Thermal grease (32) is interposed between slug (16) and under side of heat sink base (22).

USE - Used with heat sink for dissipating heat generated from electronic components.

ADVANTAGE - The interfitting of heat sink and the slug makes it possible to access the chip for testing by removing heat sink by unscrewing the heat sink from the slug. The use of slug enables easy removal of the heat sink both for **ball grid** array and non-**ball grid** array devices when it is necessary to rework such devices. Air flow between the electronic component and underside of heat sink is improved as the dimensions of the slug is less than that of the base of heat sink. The use of interfitting tongue and grooves on the base of heat sink and the top of slug, ensures proper alignment of heat sink and slug. Thermal grease interposed between slug and the underside of base, improves **thermal conductivity** from slug to the base and thereby providing proper heat dissipation.

DESCRIPTION OF DRAWING(S) - The figure shows the exploded perspective view of heat sink and heat slug.
Substrate 11
Chip 12
Slug 16
Tongue 18
Holes 19,28
Heat sink 21
Heat sink base 22
Grooves 26
Offset 27
Screws 31
Thermal grease 32
Dwg.1/3

L24 ANSWER 13 OF 34 WPIX (C) 2002 THOMSON DERWENT
AN 1999-410616 [35] WPIX
DNN N1999-306978
TI Heat dissipation structure of **BGA** semiconductor device - has through-hole in package board, which is filled with heat conduction material so as to be in **contact** with **bump** electrode of package.
DC U11
PA (HITA) HITACHI LTD

CYC 1
PI JP 11163230 A 19990618 (199935)* 7p
ADT JP 11163230 A JP 1997-324267 19971126
PRAI JP 1997-324267 19971126
AB JP 11163230 A UPAB: 19990902
NOVELTY - A semiconductor chip (2) is provided in an open hole (9) of package substrate (3). Back surface of chip and substrate are **covered** by **heat** conduction board (4). Through-hole (12) in package substrate is filled by heat conduction material for releasing heat. The through-hole is provided between bump (6) of the package and conducting board. INDEPENDENT CLAIMS are also included for the following: heat dissipation method in **BGA** package; mounting structure of **BGA** package
USE - In **BGA** semiconductor device.
ADVANTAGE - Raises heat release effect of semiconductor chip, because of filling heat conduction material in through-hole of package board so as to connect with heat conducting board and bump. Offers reduction in size of semiconductor device by avoiding usage of radiation fins. DESCRIPTION OF DRAWING(S) - The figure shows the sectional view of **BGA** semiconductor device. (2) Semiconductor chip; (3) Package board; (4) Heat conduction board; (6) Bump; (9) Open hole; (12) Through-hole.
Dwg.1/6

L24 ANSWER 14 OF 34 WPIX (C) 2002 THOMSON DERWENT
AN 1999-356858 [30] WPIX
DNN N1999-265644
TI High performance cavity-down, **ball grid** array package for integrated circuit.
DC U11
IN HAMZEHDOOST, A; MARTIN, R J
PA (VLSI-N) VLSI TECHNOLOGY INC
CYC 1
PI US 5910686 A 19990608 (199930)* 10p
ADT US 5910686 A US 1998-121792 19980723
PRAI US 1998-121792 19980723
AB US 5910686 A UPAB: 19990802
NOVELTY - A die-cavity has an insulating tape projecting into it so that the die can be bonded to the tape. The other end of the tape extends from the cavity so that conductive traces connect the wire bonding sites to solderable areas on the outer area of the tape.
DETAILED DESCRIPTION - The cavity-down HBGA integrated-circuit package for an integrated-circuit die, includes:
(1) an integrated-circuit die (112) with a die-mounting surface and a surface which has wire-**bonding pads** (114) formed on it;
(2) a die-carrier/**heat spreader** (102) which has a die-cavity (104) formed through its lower surface, where the die-mounting surface of the integrated-circuit die is attached to the top interior surface of the die-cavity, and where the die-carrier/**heat spreader** also has a lower surface outside of and surrounding the cavity;
(3) a first portion (122) of an insulated tape layer (120) which extends over the lower outside surface of the die-carrier/**heat spreader** outside of the die-cavity;
(4) the insulated tape layer also has second portions (126) which are located inside the die-cavity of the die-carrier/heat sink and which have wire-bonding sites (132) formed on them;

(5) several bonding-wire loops (140), each of which is looped between and bonded to one of the wire-**bonding pads** formed on the integrated-circuit die and a respective wire-bonding site formed on the insulated tape layer within the die-cavity to form bonding-wire loops;

(6) conductive traces (134) are formed on the insulated tape layer to connect the wire-bonding sites located inside of the die-cavity to respective selective solderable areas (137) formed on the insulated layer outside of the die-cavity;

(7) where the selective solderable areas on the insulated layer and outside of the die-cavity are arranged in a grid pattern on the bottom side of a die-down HBGA package;

(8) several solder balls (136) attached to respective selective solderable areas formed on the insulated layer outside of the die-cavity; and

(9) an encapsulation layer (150) or cover for covering and sealing the integrated-circuit die, the bonding wires, where the encapsulation layer or cover has a lower outside surface formed in it and is spaced apart from a surface to which an HBGA package is mounted.

USE - The HBGA is used for integrated circuits.

ADVANTAGE - Minimizes the thickness of the encapsulating layer while still accommodating a greater number of bonding wires, providing smaller grid spacing for smaller solder balls.

DESCRIPTION OF DRAWING(S) - The drawing shows an enlarged side sectional view of the cavity-down encapsulated HBGA package.

Die carrier/**heat spreader** 102
Die cavity 104
Integrated circuit die 112
Wire **bonding pads** 114
Insulated tape layer 120
Wire bonding sites 132
Wire bonding loops 140
Encapsulation layer 150

L24 ANSWER 15 OF 34 WPIX (C) 2002 THOMSON DERWENT
AN 1999-105338 [09] WPIX
DNN N1999-076071
TI Integrated circuit package for **BGA** - has **heat spreader** which is coupled to IC die using **thermally conductive** adhesive and has area larger than die cavity.
DC U11 V04
IN RILEY, J B
PA (NASC) NAT SEMICONDUCTOR CORP
CYC 1
PI US 5856911 A 19990105 (199909)* 6p
ADT US 5856911 A US 1996-747347 19961112
PRAI US 1996-747347 19961112
AB US 5856911 A UPAB: 19990302
The package (28) has a top cavity (30) for holding an IC die (32). The cavity is formed in a planar laminate material (29). The die is bonded with bond wires (34) to electrical traces on top of the laminate material and coupled through electrical vias to solder balls (36).

A **heat spreader** (38) is connected to the die using a **thermally conductive** adhesive and has an area larger than the cavity. A **thermally conductive** slug (40) is coupled to the **heat spreader** and spans through an opening (44) formed in the circuit board (28) where the package is placed.

USE - For PGA, SPGA.
ADVANTAGE - Maintains mechanical and thermal compatibility with existing design for TCP circuit layer. Facilitates installation and requires only standard **BGA** manufacturing equipment. Raises yield rate.
Dwg.2/5

L24 ANSWER 16 OF 34 WPIX (C) 2002 THOMSON DERWENT
AN 1999-080280 [07] WPIX
DNN N1999-057812 DNC C1999-023862
TI Connecting a **thermal spreader** to a plastic **ball grid** array - using a layer of **thermally conductive** elastic connecting medium which fills hollow structures on the connectors of the **thermal spreader**.
DC L03 P73 U11
IN CHEN, S
PA (CAES-N) CAESAR TECHNOLOGY INC
CYC 1
PI US 5851337 A 19981222 (199907)* 6p
ADT US 5851337 A US 1997-885343 19970630
PRAI US 1997-885343 19970630
AB US 5851337 A UPAB: 19990217
A **thermal** electrical enhanced **heat spreader** /slug (TEHS) (15) is connected to a plastic **ball grid** array (**PBGA**) (14) by: forming hollow structures in the connecting parts (17) of the TEHS; applying a layer of **thermally conductive** elastic connecting medium over the connecting regions of the **PBGA**; forming connections between the parts and regions, the hollow structures being filled with connecting medium; and treating the medium to form an elastic connecting structure. The connecting medium is preferably a non-metallic adhesive which is treated by UV curing, or a silver-filled resin which is treated by UV curing, or a tin solder which is treated by thermal soldering and cooling.
USE - In manufacture of **PBGA** IC packages.
ADVANTAGE - The connection between the **PBGA** substrate and the TEHS has improved contact reliability and low residual stress after connection to enhance mechanical strength and yield.
Dwg.1/3

L24 ANSWER 17 OF 34 WPIX (C) 2002 THOMSON DERWENT
AN 1998-597117 [51] WPIX
DNN N1998-464724 DNC C1998-179352
TI Thin power tape **ball grid** array package - has semiconductor chip mounted in **heat spreader** recess and its **bonding pads** connected to metal interconnect patterns on flex tape..
DC A85 L03 U11
IN ALAGARATNAM, M; CHIA, C J; VARIOT, P
PA (LSIL-N) LSI LOGIC CORP
CYC 27
PI EP 880175 A2 19981125 (199851)* EN 5p
R: AL AT BE CH CY DE DK ES FI FR GB GR IE IT LI LT LU LV MC MK NL PT RO SE SI
JP 11003957 A 19990106 (199911) 4p
US 5869889 A 19990209 (199913)
ADT EP 880175 A2 EP 1998-303039 19980421; JP 11003957 A JP 1998-109632 19980420; US 5869889 A US 1997-840614 19970421

PRAI US 1997-840614 19970421
AB EP 880175 A UPAB: 19981223
Package comprises a heat conductive support (10) formed to have a recessed portion with opposing planar surfaces (12,14) and a centrally disposed surface (16). Flex tape is attached to the planar surfaces (12,14) and extends to the centrally disposed surface (16). The flex tape includes one or more metal interconnect patterns (22) on an exposed surface. Semiconductor integrated circuit chip (24) is mounted on centrally disposed surface (16) spaced from the flex tape (18,20). Chip (24) has **bonding pads** (26). Wire bonds interconnect pads (26) to the interconnect pattern (22). Preferably chip (24) and the wire bonds are encapsulated by plastic molding or epoxy on the heat conductive support (10). Preferably the metal interconnect pattern (22) is connected by solder balls to a mother board.
USE - Flex tape **ball grid** array package where the flex tape and a formed **heat spreader** provide the package substrate.
ADVANTAGE - The use of flex tape for the substrate is cheaper to manufacture than laminates and ceramics and the wire bonding for the interconnect of the chip and the substrate is lower in cost has higher flexibility than other interconnects such as TAB bonding. The recess or cavity for attachment of the chip to the **heat spreader** allows for greater protection of the chip and easier assembly of a thin and light package.
Dwg.3/4

L24 ANSWER 18 OF 34 WPIX (C) 2002 THOMSON DERWENT
AN 1998-560253 [48] WPIX
DNN N1998-436911 DNC C1998-167831
TI **Ball grid** array (**BGA**) package for integrated circuits used in e.g. mobile telephones - has a metal **heat** sink **covered** in an insulating sheet including conductive traces, with a central hole into which is mounted the device.
DC A85 L03 U11
IN CHOI, K H; JEONG, T S; LEE, T K; PARK, J S; RYU, K T; YOUN, H S; CHOI, K; JEONG, T; LEE, T; PARK, J; RYU, K; YOUN, H; CHOI, G H; CHUNG, T S; LEE, T G; RYOO, G T; YOON, H S
PA (HYUN-N) HYUNDAI ELECTRONICS IND CO LTD
CYC 7
PI GB 2325340 A 19981118 (199848)* 72p
DE 19821715 A1 19990128 (199910)
CN 1199927 A 19981125 (199915)
JP 11045956 A 19990216 (199917) 16p
KR 98083733 A 19981205 (200007)
KR 98083734 A 19981205 (200007)
US 6060778 A 20000509 (200030)
KR 220249 B1 19990915 (200107)
TW 449844 A 20010811 (200237)
ADT GB 2325340 A GB 1998-6078 19980320; DE 19821715 A1 DE 1998-19821715 19980514; CN 1199927 A CN 1998-107932 19980506; JP 11045956 A JP 1998-100428 19980327; KR 98083733 A KR 1997-19144 19970517; KR 98083734 A KR 1997-19145 19970517; US 6060778 A US 1998-60981 19980415; KR 220249 B1 KR 1997-19144 19970517; TW 449844 A TW 1998-103626 19980312
PRAI KR 1997-19145 19970517; KR 1997-19144 19970517
AB GB 2325340 A UPAB: 19981203
An integrated circuit package comprises an interconnection substrate (50) with a conductive trace layer on each side. A first side (50b) is bonded

to a **thermally conductive** layer (35). The substrate and **thermally conductive** layer are essentially square, with a hole (36) in the centre. An integrated circuit device (40) is located in the central hole and connected to bond pads on the conductive traces on the second side of the insulating substrate before being encapsulated (42) and fixed in the hole. Solder balls connect to the conductive traces on the second side of the insulating layer. Preferably the first side of the insulating layer has an epoxy or polyimide layer around its periphery. The **thermally conductive** layer is made from aluminium silver or copper.

USE - The **ball grid** array package is used for integrated circuit devices used in portable equipment such as mobile telephones, pocket computers etc.

ADVANTAGE - The device package is low-profile, light, cheap to make and has excellent heat dissipation properties.

Dwg.3/15

L24 ANSWER 19 OF 34 WPIX (C) 2002 THOMSON DERWENT
AN 1998-238871 [21] WPIX
DNN N1998-188941 DNC C1998-074490
TI Apparatus for heating board-mounted electrical module for rework - uses heated gas to reflow all interconnection sites simultaneously and avoids component damage.
DC L03 M23 P55 V04 X24
IN HEIM, C G; LE COZ, C R; LEWIS, R H
PA (IBMC) INT BUSINESS MACHINES CORP
CYC 1
PI US 5735450 A 19980407 (199821)* 9p
ADT US 5735450 A US 1996-669902 19960621
PRAI US 1996-669902 19960621
AB US 5735450 A UPAB: 19980528

An apparatus for heating an electronic module having surface contacts attaching the module (12) to a wiring surface of a card having a planar bottom face comprises a **preheater** (16) with **cover**, opening and inlet port connected to a source of heated gas. The preheater has a heating element on a movable support (24) and contacts a **thermally conductive** plate (28) which supports a selected part of the bottom of the card (14). A nozzle (30) connected to the heated gas source contacts the wiring surface of the circuit board at a defined position and provides enclosure around the module.

Also claimed is a method of removing and replacing a module as above connected to many contact sites on a card as above comprising placing the card in the preheater, flowing the heated gas to uniformly heat the contact sites to 90-120 deg. C, contacting the nozzle to the card and flowing gas to heat the sites to solder reflow temperature. The module is removed from the card, the sites prepared for reconnection, the sites heated as above to 90-100 deg. C, an operable module aligned with the card and the nozzle and gas flow operated as before to bring the sites to a reflow temperature. Heating is then discontinued, the solder solidifies and the validated module and card are removed from the preheater.

USE - For solder reflow in reworking electronic packages such as CBGA, CCGA, **PBGA** or other SMT or QFP components

ADVANTAGE - All interconnection sites are simultaneously reflowed without damage to components or adverse effect on the solder joints. Heating times are reduced by at least 25%.

Dwg.1/4

L24 ANSWER 20 OF 34 WPIX (C) 2002 THOMSON DERWENT
AN 1997-138387 [13] WPIX
DNN N1997-114383
TI **Ball grid** array semiconductor chip - provides **thermally conductive** layer inside wiring board, connected to motherboard, and contacts semiconductor chip mounted on wiring board.
DC U11 U14
IN HIGASHIGUCHI, Y; INAGAKI, M; KUMAI, T; OCHIAI, R; TOTANI, M
PA (FUIT) FUJITSU LTD
CYC 2
PI JP 09017919 A 19970117 (199713)* 7p
US 6023098 A 20000208 (200014)
ADT JP 09017919 A JP 1995-164224 19950629; US 6023098 A US 1996-591732 19960125
PRAI JP 1995-164224 19950629
AB JP 09017919 A UPAB: 19970326
The device includes a semiconductor chip (30) supported in a wiring board (48). A **thermally conductive** layer (50) provided inside the wiring board is contacted to the semiconductor chip through a hole in the wiring board.
The wiring board is connected to a motherboard through a board terminal provided at the first wiring board surface.
ADVANTAGE - Efficiently **radiates heat** from semiconductor chip. Provides efficient heat dissipation in semiconductor chip.
Dwg.1/9

L24 ANSWER 21 OF 34 WPIX (C) 2002 THOMSON DERWENT
AN 1995-372189 [48] WPIX
DNN N1995-274310
TI Tape carrier package for **Ball Grid** Array mounting - has heat sink mounted on second pair of additional substrate which is connected to main substrate holding semiconductor chip through holes of heat conductive layer coating substrates.
DC U11
IN TAKUBO, C
PA (TOKE) TOSHIBA KK
CYC 2
PI JP 07254666 A 19951003 (199548)* 80p
US 5543663 A 19960806 (199637) 112p
JP 3056960 B2 20000626 (200035) 79p
ADT JP 07254666 A JP 1994-299048 19941109; US 5543663 A US 1994-362978 19941223; JP 3056960 B2 JP 1994-299048 19941109
FDT JP 3056960 B2 Previous Publ. JP 07254666
PRAI JP 1993-332736 19931227; JP 1993-332735 19931227
AB JP 07254666 A UPAB: 19960924
The device (102) has a semiconductor chip (15) placed on top of an electrically insulated substrate (11) coated with a heat conductive layer (21). The substrate is extended laterally with additional substrates connected to the main substrate through holes.
Only the surface of the first pair of additional substrates are coated with a heat conductive layer. The second pair of additional substrates where a heat sink is mounted is fully **covered** with **heat** conductive layer. The same heat sink mounting structure is applied for **BGA** packages mounted on a multi-layer PCB.
ADVANTAGE - Does not require heat sink to be directly mounted on

chip, preventing semiconductor chip breakage.
Dwg.0/158

L24 ANSWER 22 OF 34 WPIX (C) 2002 THOMSON DERWENT
AN 1994-340362 [42] WPIX
DNN N1994-266958
TI Fabricating IC packages from laminated boards and **heat spreader** e.g for mfg. PPGA and **PBGA** IC packages - laminating planar metal sheet to printed wiring boards, cutting sheet into sections resulting in individual packages, and placing integrated circuit dies in cavity of each package.
DC U11 V04
IN NEWMAN, K G
PA (LSIL-N) LSI LOGIC CORP
CYC 1
PI US 5357672 A 19941025 (199442)* 12p
ADT US 5357672 A US 1993-106026 19930813
PRAI US 1993-106026 19930813
AB US 5357672 A UPAB: 19941212
The method involves laminating a number of panels of printed wiring boards to a metal panel, and forming in the laminated printed wiring board panels a number of cavities for receiving integrated circuit dice having connection pads. The printed wiring boards of the laminated panels have **contact pads** connected to a predetermined conductive path, and the printed wiring boards have external connections connected to conductive paths other than the predetermined conductive paths. Related conductive paths connected to the **contact pads** of the printed wiring boards and the external connections of the printed wiring boards are interconnected.

An integrated circuit dice having connection pads is placed into each of the number of cavities and the integrated circuit dice connection pads are attached to the respective printed wiring board **contact pads**. Sections of the metal panel and printed wiring board panels are cut into individual integrated circuit packages.

ADVANTAGE - Minimises mfg. waste by detecting defective planar substrate assemblies before attachment to **heat spreader** panel. Minimises fabrication steps, improves coplanarity of IC package, improves **thermal conductivity** and heat dissipation of IC package. Improves ease of adding discrete components e.g by-pass capacitors and removal of unwanted solder flux.
Dwg.2/8

L24 ANSWER 23 OF 34 JAPIO COPYRIGHT 2002 JPO
AN 2001-102505 JAPIO
TI ASSEMBLING METHOD FOR CIRCUIT BOARD
IN KAWAMATA TETSUJI; YATSUGI FUMISHIGE
PA HITACHI LTD
PI JP 2001102505 A 20010413 Heisei
AI JP 1999-278124 (JP11278124 Heisei) 19990930
PRAI JP 1999-278124 19990930
SO PATENT ABSTRACTS OF JAPAN (CD-ROM), Unexamined Applications, Vol. 2001
AB PROBLEM TO BE SOLVED: To effectively cool a module at an inexpensive cost, when the module is made into a circuit board on which a bear chip is directly assembled and the module is assembled on the circuit board by a **ball grid** array to make a compound circuit board.
SOLUTION: A compound circuit board 2, on which a module 4 on which a bear chip IC5 is assembled directly is mounted by a ball grit array 6, is

provided with the module 4 and the **ball grid** array 6 being **covered** by **thermal conductive** resin 3 containing a filler such as ceramics. By a means for cooling for the module 4 and reinforcement for the **ball grid** array 6 are realized.
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L24 ANSWER 24 OF 34 JAPIO COPYRIGHT 2002 JPO
AN 2000-294678 JAPIO
TI PRINTED WIRING BOARD FOR HIGH **HEAT RADIATION** **BALL GRID** ARRAY TYPE SEMICONDUCTOR PLASTIC PACKAGE
IN KANEHARA HIDENORI; IKEGUCHI NOBUYUKI; KOMATSU KATSUJI
PA MITSUBISHI GAS CHEM CO INC
PI JP 2000294678 A 20001020 Heisei
AI JP 1999-98065 (JP11098065 Heisei) 19990405
PRAI JP 1999-98065 19990405
SO PATENT ABSTRACTS OF JAPAN (CD-ROM), Unexamined Applications, Vol. 2000
AB PROBLEM TO BE SOLVED: To provide a printed wiring board for a **BGA** type semiconductor plastic package excellent in **heat radiation, heat** resistance, electrical insulation after moisture absorption, migration resistance, and the like.
SOLUTION: A circuit c is formed on at least one side of a glass fabric base double-sided copper-clad laminate, a glass fabric base prepreg d is put on the circuit after surface treatment, a copper foil a or a glass fabric base single sided copper-clad laminate is formed outside and laminated with being heated and pressed, and a printed wiring board is made by cutting and removing an internal layer **bonding pad** part, a glass fabric base on the back side of copper foil which will be a semiconductor chip mounting section, and a thermosetting resin composition by the sandblasting method and plating noble metal. Multifunctional ester resin cyanate composition is used as resin of the copper- clad laminate and the prepreg. The printed wiring board excellent in **heat radiation, heat** resistance, electrical insulation after pressure cooker treatment, migration resistance, and suitable for high volume production can be obtained.
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L24 ANSWER 25 OF 34 JAPIO COPYRIGHT 2002 JPO
AN 2000-174186 JAPIO
TI SEMICONDUCTOR DEVICE AND METHOD FOR MOUNTING THE SAME
IN YAMAGUCHI EIJI; KIKUCHI TAKU
PA HITACHI LTD
PI JP 2000174186 A 20000623 Heisei
AI JP 1998-348146 (JP10348146 Heisei) 19981208
PRAI JP 1998-348146 19981208
SO PATENT ABSTRACTS OF JAPAN (CD-ROM), Unexamined Applications, Vol. 2000
AB PROBLEM TO BE SOLVED: To avoid lowering of mounting workability and wiring density of a mounting board for raised **heat-radiation** performance.
SOLUTION: **BGA**.LSI comprises a wiring board 20 where a chip 10 is CCBed(controlled collapse bonding), a **heat-radiation** fin 30 coated on the wiring board 20, a **thermal conductive** material layer 19 formed between the **heat-radiation** fin 30 and the chip 10, a stopper 33 which, protruded below the lower surface of the **heat-radiation** fin 3, hits the upper surface of the wiring board 20, and a leaf spring 35 which connects the **heat-radiation** fin 30 and the wiring

board 20, with the wiring board 20 CCBed to a mounting board 40 with a connection terminal 45 of a solder bump. Since the **heat-radiation** fin is positioned on the wiring board by a stopper, the thickness of **thermal conductive** material layer is kept constant for its stable **thermal conductivity** capability, so no hole is required to be opened on the mounting substrate wherein a specified **heat- radiation** performance is assured at all trmes, avoiding lowering of mounting workability and wiring density of the mounting board.
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L24 ANSWER 26 OF 34 JAPIO COPYRIGHT 2002 JPO
AN 2000-068411 JAPIO
TI SEMICONDUCTOR PLASTIC PACKAGE
IN TAKE MORIO; IKEGUCHI NOBUYUKI; KOBAYASHI TOSHIHIKO
PA MITSUBISHI GAS CHEM CO INC
PI JP 2000068411 A 20000303 Heisei
AI JP 1998-250445 (JP10250445 Heisei) 19980820
PRAI JP 1998-250445 19980820
SO PATENT ABSTRACTS OF JAPAN (CD-ROM), Unexamined Applications, Vol. 2000
AB PROBLEM TO BE SOLVED: To provide a semiconductor plastic package with superior connection between an inner-layer metal core and an outer layer metal foil, **heat radiation, heat** resistance, after moisture absorption, etc.
SOLUTION: In a semiconductor plastic package with a **ball grid** array using both-sided truncated conical metal cores with both surfaces, truncated conical protrusions on the front surface and the rear surface are individually exposed between semiconductor chip mounted metal foils a and between metal foils for ball pads, respectively. After a desmearing treatment of the exposed metal surfaces, the entire surfaces are metal-plated and coated with a plating resist, excluding a semiconductor chip mounting part g, the **bonding pad** parts and ball pad parts. In the printed wiring board obtained by plating with a noble metal h, a metal core c and a through-hole f are insulated by a thermosetting resin composition such as multifunctional cyanate ester, etc. A semiconductor chip is fastened on one surface of the wiring board with a heat-conductive adhesive and the chip, wires and **bonding pads** are resin-sealed in this semiconductor plastic package.
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L24 ANSWER 27 OF 34 JAPIO COPYRIGHT 2002 JPO
AN 1999-214566 JAPIO
TI SEMICONDUCTOR PLASTIC PACKAGE
IN TAKE MORIO; IKEGUCHI NOBUYUKI; YAMANE KOZO
PA MITSUBISHI GAS CHEM CO INC
PI JP 11214566 A 19990806 Heisei
AI JP 1998-11528 (JP10011528 Heisei) 19980123
PRAI JP 1998-11528 19980123
SO PATENT ABSTRACTS OF JAPAN (CD-ROM), Unexamined Applications, Vol. 1999
AB PROBLEM TO BE SOLVED: To obtain a semiconductor plastic package whose **heat radiation** and **heat** resistance after moisture absorption or the like are excellent.
SOLUTION: This is a semiconductor plastic package of a **ball grid** array using a metal core print wiring board. One part of a metal core is exposed at one part of the front and back surfaces, and a semiconductor chip fixed on the exposed metal pat on the surface and the surrounding circuit conductor are connected by wire bonding. A front and

back circuit insulated by a thermosetting resin composition with the metal core is conducted by a through-hole conductor insulated through the thermosetting resin composition with the metal core having a slit hole, and one or more through-holes are directly connected with the metallic core, and the semiconductor chip, wire, and **bonding pad** are resin sealed.
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L24 ANSWER 28 OF 34 JAPIO COPYRIGHT 2002 JPO
AN 1999-214563 JAPIO
TI SEMICONDUCTOR PLASTIC PACKAGE
IN TAKE MORIO; IKEGUCHI NOBUYUKI; YAMANE KOZO
PA MITSUBISHI GAS CHEM CO INC
PI JP 11214563 A 19990806 Heisei
AI JP 1998-9568 (JP10009568 Heisei) 19980121
PRAI JP 1998-9568 19980121
SO PATENT ABSTRACTS OF JAPAN (CD-ROM), Unexamined Applications, Vol. 1999
AB PROBLEM TO BE SOLVED: To obtain a semiconductor plastic package whose **heat radiation** and **heat** resistance after moisture absorption or the like is excellent.
SOLUTION: This is a semiconductor plastic package of a **ball grid** array using a metal core print wiring board. One part of a metal core is exposed at one part of the front and back surfaces, and a semiconductor chip fixed on the exposed metal part on the surface and the surrounding circuit conductor are connected through wire bonding. A front and back circuit insulated through a thermosetting resin composition with the metal core is conducted by a through-hole conductor insulated through the thermosetting resin composition with the metal core having a slit hole, and the metal core exposed part on the back face is used for **heat radiation**, and the semiconductor chip, wire, and **bonding pad** are resin sealed.
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L24 ANSWER 29 OF 34 JAPIO COPYRIGHT 2002 JPO
AN 1999-214562 JAPIO
TI SEMICONDUCTOR PLASTIC PACKAGE
IN TAKE MORIO; IKEGUCHI NOBUYUKI; YAMANE KOZO
PA MITSUBISHI GAS CHEM CO INC
PI JP 11214562 A 19990806 Heisei
AI JP 1998-9567 (JP10009567 Heisei) 19980121
PRAI JP 1998-9567 19980121
SO PATENT ABSTRACTS OF JAPAN (CD-ROM), Unexamined Applications, Vol. 1999
AB PROBLEM TO BE SOLVED: To obtain a semiconductor plastic package whose **heat radiation** and **heat** resistance after moisture absorption or the like is excellent.
SOLUTION: This is a semiconductor plastic package of a **ball grid** array using a metallic core print wiring board. One part of a metallic core is exposed at one part of the front and back surfaces, and a semiconductor chip fixed on the exposed metallic part on the surface and the surrounding conductor are connected through wire bonding. A front and back circuit insulated through a thermosetting resin composition with the metallic core is conducted by a through-hole conductor insulated with the metallic core, and the metallic core exposed part on the back face is used for **heat radiation**, and the semiconductor chip, wire, and **bonding pad** are resin sealed. Thus, a semiconductor plastic package whose **heat radiation** and **heat** resistance after moisture absorption is excellent in a new

structure suitable for mass productivity can be obtained.
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L24 ANSWER 30 OF 34 JAPIO COPYRIGHT 2002 JPO
AN 1999-204685 JAPIO
TI SEMICONDUCTOR PLASTIC PACKAGE
IN TAKE MORIO; IKEGUCHI NOBUYUKI; YAMANE KOZO
PA MITSUBISHI GAS CHEM CO INC
PI JP 11204685 A 19990730 Heisei
AI JP 1998-4835 (JP10004835 Heisei) 19980113
PRAI JP 1998-4835 19980113
SO PATENT ABSTRACTS OF JAPAN (CD-ROM), Unexamined Applications, Vol. 1999
AB PROBLEM TO BE SOLVED: To provide a semiconductor plastic package having superior **heat radiation** performance and **heat** resistance after absorption of moisture.
SOLUTION: This semiconductor plastic package of **ball grid** array type uses a metal core printed wiring board, and metal core projections are exposed outside on a part of top and bottom surfaces. A semiconductor chip, fixed to the metal core projection on the top surface, is wire-bonded to a circuit conductor around the chip, and the circuits on the top and bottom surfaces are connected via a through-hole and **heat** is **radiated** from the metal core projection exposed on the bottom surface. At least a semiconductor chip, the wiring, and a **bonding pad** are encapsulated by resin. This semiconductor plastic package obtained has superior **heat radiation** performance and **heat** resistance after the absorption of moisture and is suitable for mass production.
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L24 ANSWER 31 OF 34 JAPIO COPYRIGHT 2002 JPO
AN 1999-204675 JAPIO
TI **BGA** PACKAGE
IN MATSUOKA MASANARI
PA PFU LTD
PI JP 11204675 A 19990730 Heisei
AI JP 1998-5091 (JP10005091 Heisei) 19980113
PRAI JP 1998-5091 19980113
SO PATENT ABSTRACTS OF JAPAN (CD-ROM), Unexamined Applications, Vol. 1999
AB PROBLEM TO BE SOLVED: To reduce inductance and/or improve **heat radiation** property through formation of a short power supply line by providing a power supply terminal as the power supply electrode in the neighborhood of a boding pad as the power supply electrode of a semiconductor chip, and then connecting such power supply terminal to the **bonding pad**.
SOLUTION: A power supply terminal 1 as a power supply electrode is provided in an the neighborhood of a **bonding pad** 3 as the power supply electrode of a semiconductor chip 2 and is then connected to the **bonding pad**. Or the power supply terminal 1 is provided adjacent to the **bonding pad** 3 as the power supply electrode in an active area of the semiconductor chip 2 and then connected in the shortest distance. Alternatively the power supply terminal 1 is connected to a matrix type power supply conductor 11 provided in the active area of the semiconductor chip 2. As explained above, a short power supply line can be formed by setting power supply terminal provided in addition to the terminal group such as signals, and a **BGA** package of the structure having reduced power supply noise by a low inductance can be attained.

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L24 ANSWER 32 OF 34 JAPIO COPYRIGHT 2002 JPO
AN 1999-067968 JAPIO
TI **BALL GRID** ARRAY PACKAGE, MANUFACTURE THEREOF AND PRINTED CIRCUIT BOARD THEREFOR
IN AN INTETSU; KA YUKI; RI EIBIN
PA SAMSUNG ELECTRON CO LTD
PI JP 11067968 A 19990309 Heisei
AI JP 1998-49245 (JP10049245 Heisei) 19980302
PRAI KR 1997-38466 19970812
SO PATENT ABSTRACTS OF JAPAN (CD-ROM), Unexamined Applications, Vol. 1999
AB PROBLEM TO BE SOLVED: To avoid moisture absorption through **heat radiating** vias and improve **heat radiation**, by filling these vias with a metal having a high **thermal conductivity** and low moisture absorption.
SOLUTION: A package 200 comprises a printed circuit board 110 having a chip mounting region 160 and a circuit pattern 15, a semiconductor chip mounted on the mounting region 160, bonding wires 140 for electrically connecting the semiconductor chip to a circuit pattern 115, a package body 150 formed with the sealed semiconductor chip and the bonding wires 140, and solder balls 130. **Heat radiating** vias 162a are formed in a lower part of the chip-mounting region 160 to **radiate** out the **heat** generated during operating of the chip and filled with a low-m.p. metal 172 to avoid penetrating the water content in the package body, and to improve the **heat radiation**.
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L24 ANSWER 33 OF 34 JAPIO COPYRIGHT 2002 JPO
AN 1999-003957 JAPIO
TI THIN-FILM POWER TAPE **BALL GRID** ARRAY PACKAGE
IN CHIA CHOK J; VARIOT PATRICK; ALAGARATNAM MANIAM
PA LSI LOGIC CORP
PI JP 11003957 A 19990106 Heisei
AI JP 1998-109632 (JP10109632 Heisei) 19980420
PRAI US 1997-840614 19970421
SO PATENT ABSTRACTS OF JAPAN (CD-ROM), Unexamined Applications, Vol. 1999
AB PROBLEM TO BE SOLVED: To provide a **ball grid** array package which is economical and high in its density.
SOLUTION: An integrated circuit package 2 includes a **heat spreader** 4 formed to have a central recess face 16 between its flat faces 12 and 14, and also includes flexible tapes extended from the flat faces 12 and 14 to the central recess face 16. A semiconductor chip 24 is mounted on the central recess face 16 between the flexible tapes and then, by wire **bonding**, the **bonding pads** of the chip 24 are interconnected to a metal interconnect pattern of the tapes. Then plastic molding or epoxy is applied to seal the chip and wire bonding on the central recess face of the **heat spreader** 4. Thereby the package 2 can be easily mounted on a motherboard by means of solder balls.
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L24 ANSWER 34 OF 34 JAPIO COPYRIGHT 2002 JPO
AN 1998-247702 JAPIO
TI **BALL GRID** ARRAY PACKAGE AND PRINTED BOARD
IN FUKUNAGA NORIKAZU
PA SUMITOMO KINZOKU ELECTRO DEVICE:KK

PI JP 10247702 A 19980914 Heisei
AI JP 1997-69157 (JP09069157 Heisei) 19970305
PRAI JP 1997-69157 19970305
SO PATENT ABSTRACTS OF JAPAN (CD-ROM), Unexamined Applications, Vol. 1998
AB PROBLEM TO BE SOLVED: To improve the **heat radiating** property, by a method wherein a **heat radiating** board in excellent **thermal conductivity** is junctioned with the bottom face side of the semiconductor element mounting part of a resin substrate having the semiconductor element mounting part on the top face side, with the junctioning pad of a solder ball on the bottom face side. SOLUTION: A **ball grid** array package 10 is provided with a resin substrate 13 having the mounting part of a semiconductor element 11 on the top face side thereof while having a solder ball junctioning pad on the bottom face side thereof. On the other hand, a **heat radiating** board 21 in excellent **thermal conductivity** is junctioned with the bottom face side of the semiconductor element mounting part of the resin substrate 13. Resultantly, the heat dissipated from the bottom face of the semiconductor element 1 is radiated to a printed substrate 41 in almost the shortest distant path. Besides, the **heat radiating** board 21 formed of a material in excellent **thermal conductivity** such as copper, etc., also takes a planar shape at the lower thermal resistance, thereby enabling the semiconductor element 11 to efficiently **radiate** the **heat** to the printed wiring board 4

L31 ANSWER 1 OF 2 WPIX (C) 2002 THOMSON DERWENT
AN 2001-366595 [38] WPIX
CR 2001-122266 [08]
DNN N2001-267416 DNC C2001-112393
TI Packaging microcircuits with pads and lead extensions, first adheres leads to substrate facilitating heat dissipation, then makes electrical bonds from pads to leads.
DC A85 L03 U11
IN BRIAR, J; **ZHANG, T**
PA (STAS-N) ST ASSEMBLY TEST SERVICES PTE LTD
CYC 1
PI US 2001002320 A1 20010531 (200138)* 7p
ADT US 2001002320 A1 Div ex US 1998-104031 19980624, US 2000-726260 20001130
PRAI US 1998-104031 19980624; US 2000-726260 20001130
AB US2001002320 A UPAB: 20010711
NOVELTY - Semiconductor circuit substrate (28) has pads (29) e.g. on top. An extended lead (24) is bonded (32) below the circuit substrate, the bond being thermally- but not electrically conductive. An electrical connection (30) is completed between pad and lead.

DETAILED DESCRIPTION - An INDEPENDENT CLAIM is included for the package so formed.

USE - To make an extended lead package.

ADVANTAGE - When conventional lead frame connection is used, a **thermal spreader** or slug may be required on the back of the package, to dissipate heat, involving additional cost and complexity. The new design avoids or supplements this measure, improving heat dissipation. The method is suitable for standard fabrication and encapsulation techniques.

DESCRIPTION OF DRAWING(S) - The drawing shows a schematic cross section of a single lead and part of the substrate.

extended lead 24

semiconductor circuit substrate 28

pads 29

electrical connection 30

bond 32

Dwg.5/7

L31 ANSWER 2 OF 2 WPIX (C) 2002 THOMSON DERWENT
AN 2000-665775 [65] WPIX
DNN N2000-493355
TI Combined multifunctional speed-varying burner.
DC Q73 X27
IN **ZHANG, T**
PA (ZHAN-I) ZHANG T
CYC 1
PI CN 1265454 A 20000906 (200065)*
ADT CN 1265454 A CN 1999-113136 19990730
PRAI CN 1999-113136 19990730
AB CN 1265454 A UPAB: 20001214
NOVELTY - The combined multifunctional speed-changing burner is designed to be used in rotary kiln burning various coal with different features and heat value. Unlike available single and three air duct coal sprayer inapplicable for coal variety change, the burner of the present invention has several air ducts of different aperture, a primary wind temperature regulating system and a flame stabilizing systemand thus can be regulated in air-coal ratio and spray speed and controlled in **thermal**

condition, **radiation** space, etc.without changing flame shape. The burner can result in high yield and quality ofrotary kiln. Dwg.0/0